HIGH ASPECT-RATIO NANOSCALE ETCHING IN SILICON USING ELECTRON BEAM LITHOGRAPHY AND DEEP REACTIVE ION ETCHING (DRIE) TECHNIQUE

A Dissertation
Presented to
The Academic Faculty

by

John Kangchun Perng

In Partial Fulfillment
Of the Requirements for the Degree
Master of Science in the
School of Electrical Engineering

Georgia Institute of Technology

August 2006

HIGH ASPECT-RATIO NANOSCALE ETCHING IN SILICON USING ELECTRON BEAM LITHOGRAPHY AND DEEP REACTIVE ION ETCHING (DRIE) TECHNIQUE

Approved by:

Dr. Farrokh Ayazi, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Bruno Frazier
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Oliver Brand
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: June 23, 2006

This work is dedicated to my dear grandmother, who has not only taught me that learning is a life-long matter, but has also inspired me by being an example herself even at the age of 80.

ACKNOWLEDGEMENTS

I would like to thank my advisor and mentor, Dr. Farrokh Ayazi, whose support and guidance has provided this work. I also like to acknowledge the following people for their help: Raghu Murali and Devin Brown for the training on the Electron Beam Lithography system; Reza Abdolvand and Siavash Pourkamali for the help on fabrication; Gavin Ho and Dr. Julie Hao for the help on design and modeling; and all the members of the IMEMS group for creating a collaborative and pleasant atmosphere. Special thanks to all the MiRC Cleanroom staff, who I am greatly indebted to, for all of their dedication, hard work, and always bearing with me on many technical questions.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

This thesis reports the characterization and development of nanolithography using Electron Beam Lithography system and nanoscale plasma etching. The standard Bosch process and a modified three-pulse Bosch process were developed in STS ICP and Plasma ICP system separately. The limit of the Bosch process at the nanoscale regime was investigated and documented. Furthermore, the effect of different control parameters on the process were studied and summarized in this report. 28nm-wide trench with aspect-ratio of 25 (smallest trench), and 50nm-wide trench with aspect ratio of 37 (highest aspect-ratio) have been demonstrated using the modified three-pulse process.

Capacitive resonators, SiBAR and IBAR devices have been fabricated using the process developed in this work. IBARs (15MHz) with ultra-high Q (210,000) have been reported.

CHAPTER 1

INTRODUCTION

Silicon MEMS resonators have many potential in RF and sensing applications, including filter, reference oscillator and biosensor. The advantages of using silicon as the structural material for MEMS resonator include high mechanical quality factor, miniaturization, compatibility with integrated circuit technology, well-developed tools for batch-fabrication, and long term stability.

In order to increase the sensitivity of capacitive resonators, the electro-mechanical coupling must be enhanced. This can be accomplished by either reducing the electrode gap size, or increasing the electrode area, or both. However, as the size of the resonator continues to shrink at higher operating frequency (>1GHz), the area available for the electrode becomes limited. Therefore, it is more favorable to decrease the size of the electrode gap in high frequency devices.

One method of creating small electrode gap is through the HAPRSS process (High Aspect-Ratio Poly and Single-crystal Silicon), in which a thin layer of sacrificial oxide is deposited between the electrode and the body of the resonator. This sacrificial oxide is removed at the end of the process to produce the electrode gap. This technique has yielded an 80nm-wide gap with an aspect ratio of 250. The other method is to pattern small feature with advanced lithography tool, such as Electron Beam Lithography, and etch the trench directly into the silicon substrate.

The objective of this research is to develop and characterize high aspect-ratio nanoscale trench etching technology in silicon substrate. In particular, nanolithography

using the Electron Beam Lithography system and plasma etching based on the Bosch process are the focus of this investigation.

This thesis is organization into six chapters:

Chapter 1 gives the introduction.

Chapter 2 provides the background and motivation for gap-reduction in MEMS capacitive resonator.

Chapter 3 presents the basic design and modeling of capacitive resonator.

Chapter 4 presents the development and characterization results of the nanolithography process.

Chapter 5 provides the characterization of process parameter and results of nanoscale plasma etching.

Chapter 6 shows measurement results of fabricated resonator devices.

Chapter 7 concludes the work and suggests future application.

CHAPTER 2

BACKGROUND AND MOTIVATION

2.1 MEMS resonator

Micro-electro-mechanical (MEM) resonator is a micromachined mechanical structure with integrated transducers that can convert the motion of a micromechanical element into electrical signal and vice-versa. There are many different transduction mechanisms, such as piezoelectric, capacitive, thermal and magnetostrictive [1]. The MEM resonator has at least one high quality factor (Q) resonant mode that can be excited using the transducers. The quality factor of a resonator is defined as the resonant frequency divided by its 3dB bandwidth:

$$Q = \frac{f_{resonance}}{BW_{-3dB}}$$

The smaller the -3dB bandwidth of the resonance is, the higher the Q of the resonator is. Another definition of the quality factor Q is give by:

$$Q = 2\pi \times \frac{peak\_energy\_stored}{energy\_dissipated\_per\_cycle}$$

Thus, in order to obtain high Q in micromechanical resonators, energy dissipation through various loss mechanisms should be minimized.

Capacitive signal transduction does not require any physical contact between the electrodes and the resonating body, and therefore, it can yield much higher mechanical quality factor (~100,000) compare to other transduction mechanisms. An example of a

two-port capacitive resonator, in which the micromechanical resonator is a clamped-clamped silicon beam designed to operate in its in-plane bending flexural mode is given in Figure 2.1

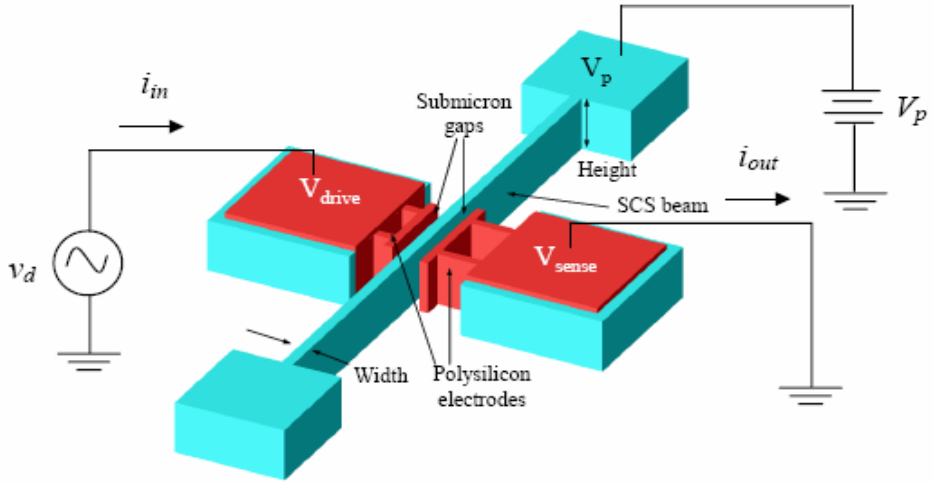


Figure 2.1: Operating configuration of a two-port clamped-clamped capacitive beam resonator

In this schematic, a DC bias voltage V_p is applied to the body of the beam while the DC levels of the drive and sense electrodes are set to ground. In order to excite the beam into resonance, an AC drive signal v_d is applied to the drive electrode, and the sense current i_s from the sense electrode is measured. The sense current i_s is a measure of the vibration amplitude of the micromechanical beam, and it is amplified by the Q factor of the resonator at its resonance frequency.

In order to sense very small vibration, a large electro-mechanical coupling between the electrode and the resonating body is required. This can be improved by having a large sense capacitance to reduce the motional resistance. The equivalent electrical output resistance of a capacitive micromechanical resonator is expressed by the equation:

$$R_m = \frac{\sqrt{KM}\,d^4}{Q\varepsilon_o{}^2 L^2 h^2 V_p{}^2} \propto \frac{d^4}{Q \cdot h}$$

Where K and M are the effective stiffness and mass of the resonator, d is the capacitive gap size, Q is the resonator's quality factor, V_p is the DC bias voltage, ε_o is the permittivity of vacuum, and L and h are the electrode's length and height. From this equation, it can be seen that the motional resistance can be reduced by having small capacitive gaps, high Q, and large electrode area.

However, as the size of the resonator scales down to a few microns to reach high operating frequency (>1GHz), the area available for the electrode is limited. Furthermore, even though the sensitivity scales linearly with a larger capacitive area, the sensitivity scales up to the fourth power with decreasing gap size. Hence, it is more favorable to reduce the gap size in order to increase the overall sensitivity. For this reason, different fabrication technologies have been developed to achieve high aspect-ratio sub-100nm gap in silicon. In this work, two gap reduction methods are presented and compared.

2.2 Gap reduction technique – HARPSS (High Aspect-Ratio Poly and Single-crystalline Silicon process)

The HAPRSS process (High Aspect-Ratio Poly and Single-crystalline Silicon) is a fabrication technology that has been developed in our group to produce precision micromachined inertial sensors [2, 3, 4]. It is capable of producing 10-100's of microns thick silicon microstructures. The key advantage of using a thin sacrificial oxide layer to define the electrode gap is that the gap size can be reduced to sub-micron level. High-Q

single crystalline silicon resonators with 80nm-wide electrode gap on 20um-thick substrate (aspect-ratio 250) have been demonstrated using this process [5]. Figure 2.2 shows the top view of a 150MHz silicon disk resonator with 80nm electrode gap space. These resonators were fabricated by Siavash Pourkamali.

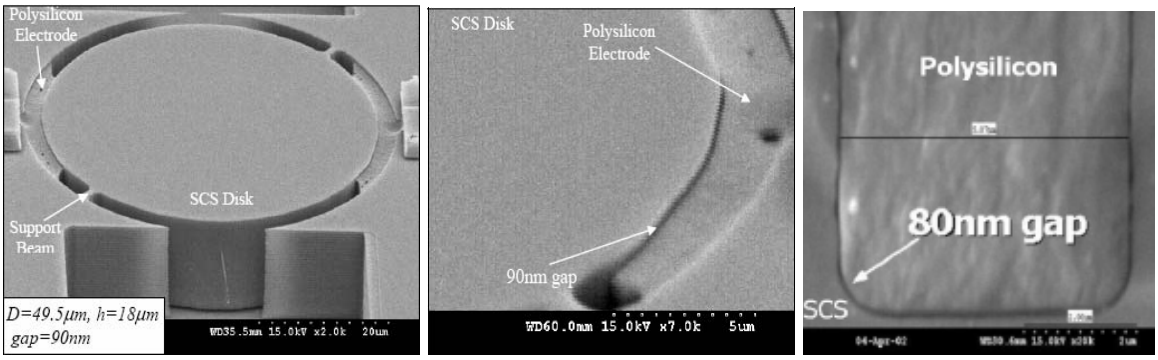


Figure 2.2: 150MHz silicon disk resonator with 80nm-wide electrode gap and aspect-ratio of 250

The basic fabrication process starts with growing a thermal oxide layer on top of low resistivity SOI (silicon on insulator) wafer. The oxide is patterned and kept only on top of the body of the resonator and the wire-bonding pads. The oxide layer serves as an etching mask to protect the silicon structure underneath against silicon and poly-silicon etching in later steps. Next, vertical trenches are etched down to the buried oxide layer to define the shape of the resonator in the silicon device layer. A thin layer of LPCVD sacrificial oxide is deposited inside the trench. The thickness of the LPCVD oxide determines the electrode gap spacing between the body of the resonator and its electrodes. Since the oxide thickness is independent of the optical lithographic limit, the gap size can be as few as tens of nanometer. The sacrificial oxide is etched back on the surface, and the trench is refilled with highly-doped poly-silicon to form the electrodes. The poly-silicon inside the trench is patterned and kept only in the electrode area. The

final structure is released in hydrofluoric acid by removing the sacrificial oxide inside the electrode gap and the buried oxide underneath. Figure 2.3 illustrates the HARPSS process flow.

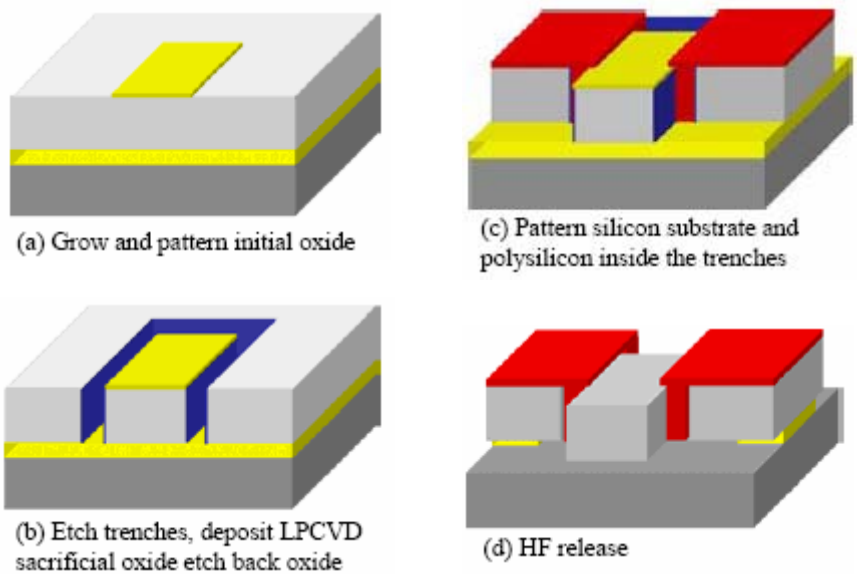


Figure 2.3: HAPRSS process flow

However, the HARPSS process requires multiple photolithography masks and optical alignment. The current minimum resolution of the photolithography tool in our cleanroom facility is 1um, which limits the alignment accuracy for sub-micron feature. Furthermore, other technical challenges exist, such as void formation during the trench-refill step, and etching the poly-silicon inside the electrode gap. All of these issues degrade the quality of the resonator. Therefore, alternative method needs to be developed to circumvent these problems.

2.3 Gap reduction technique – Nanolithography

Nanolithography using electron beam lithography can pattern small feature with 4nm resolution. It does not require any photolithography masks or optical alignment. Electron beam lithography is a great tool for research and development because of its versatility and quick design and test cycle time. When a new idea is conceived, the layout can be drawn, and the device can patterned, fabricated and tested in the matter of a couple days. This greatly reduces the cost of mask-making, shortens the design cycle time, and avoids making unnecessary mistake before a final design is made on a large mask.

In this work, electron beam lithography and deep-reactive-ion plasma etching (DRIE) are used to investigate high aspect-ratio silicon trench etching at the nanometer scale. In particular, the limit of scaling down the Bosch silicon etching process at the nano-domain is studied. Figure 2.4 illustrates the process flow of nanolithography and nano etching.

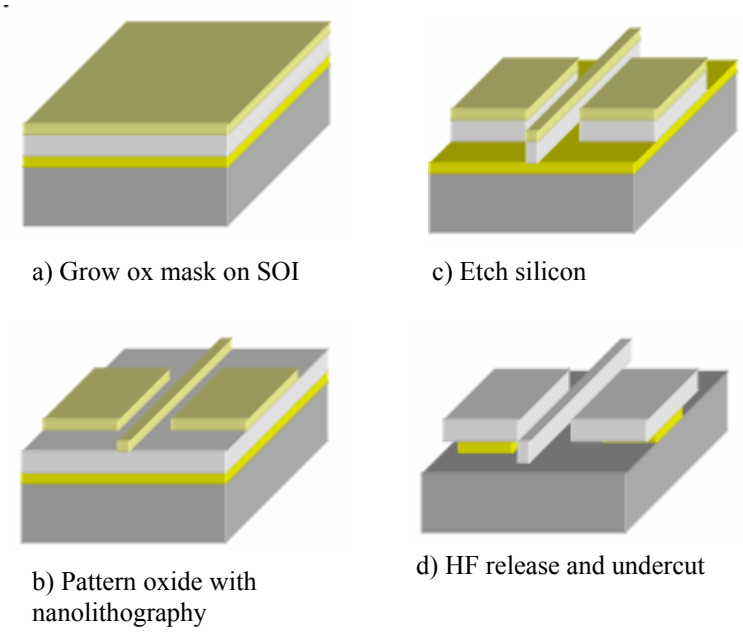


Figure 2.4: Process flow of nanolithography and nano etching

CHAPTER 3

RESONATOR DESIGN AND MODELING

Physical structures have mechanical resonances that occur at specific frequencies. The shape and frequency of these resonances depend on the clamping condition, the effective mass (M_{eff}), and the stiffness (K_{eff}) of the structure. The resonant frequency is given by the following equation:

$$\omega_{resonance} = 2\pi f = \sqrt{\frac{K_{eff}}{M_{eff}}}$$

Mechanical resonant modes of a structure can have various shapes and stiffness. High aspect-ratio structures have low-stiffness bending flexural mode as well as high-stiffness extensional modes, depending on the clamping condition. In this work, three types of resonator designs have been used. They are beam resonator, SiBAR (silicon bulk acoustic resonator), and IBAR.

3.1 Beam resonator

Micromachined beam resonators are of great interest for a wide range of sensing and frequency filtering applications. The vibration of a beam resonator can be calculated using the well-established beam theory [6]. The resonant frequency of a beam resonator is given by the following equation:

$$f = \frac{\pi B^2 W}{2L^2}\sqrt{\frac{E}{12\rho}}$$

Where *f* denotes the resonant frequency, *B* is the mode constant, *W* and *L* is the width and length of the beam, *E* is the Young's modulus of the material, and ρ is the density of the material. An applied polarization voltage on the body of the resonator is necessary for normal operation. However, the polarization voltage cannot exceed the pull-in voltage; otherwise, the resonator will not operate in its linear region. The equation for pull-in voltage is given by:

$$V_{pull-in} = \sqrt{\frac{8Kd^3}{27A\varepsilon_o}}$$

Where *K* denotes the effective stiffness, *A* denotes the electrode area, *d* denotes the electrode gap, and ε_o denotes the permittivity of vacuum.

In order to decrease the motional resistance, the electrode gap size needs to be reduced. Table 3.1 shows the design of a 20um x 1um beam resonator with various electrode gap sizes.

Table 3.1: 20um x 1um beam resonator with various electrode gap sizes

Vp (V)	Length (um)	Width (um)	Height (um)	Gap (nm)	Rm (Ω)	AR	Current (A)	Frequency (Hz)
20	20	1	2	200 nm	206K Ω	10	0.06uA	19MHz
20	20	1	2	100 nm	13K Ω	20	0.12uA	19MHz
20	20	1	2	50 nm	808 Ω	40	0.25uA	19MHz
20	20	1	2	25 nm	51 Ω	80	0.49uA	19MHz

For many RF and wireless communication application, a 50Ω motional resistance is required for impedance matching. From Table 3.1, one could see that ultra-small gap with ultra-high aspect-ratio are required to achieve this.

3.2 SiBAR/block resonator

SiBAR (silicon bulk acoustic resonator) or block resonator operates in the extensional mode. The resonant frequency of a SiBAR is given by the following equation:

$$f = n\frac{\sqrt{E/\rho}}{2W}$$

Where f denotes the resonant frequency, n is the order of the resonant mode, W is the width of the block, E is the Young's modulus of the material, and ρ is the density of the material. ANSYS simulations of the mode shapes of a 105MHz SiBAR are shown in Figure 3.1. The ANSYS simulations are provided by Gavin Ho.

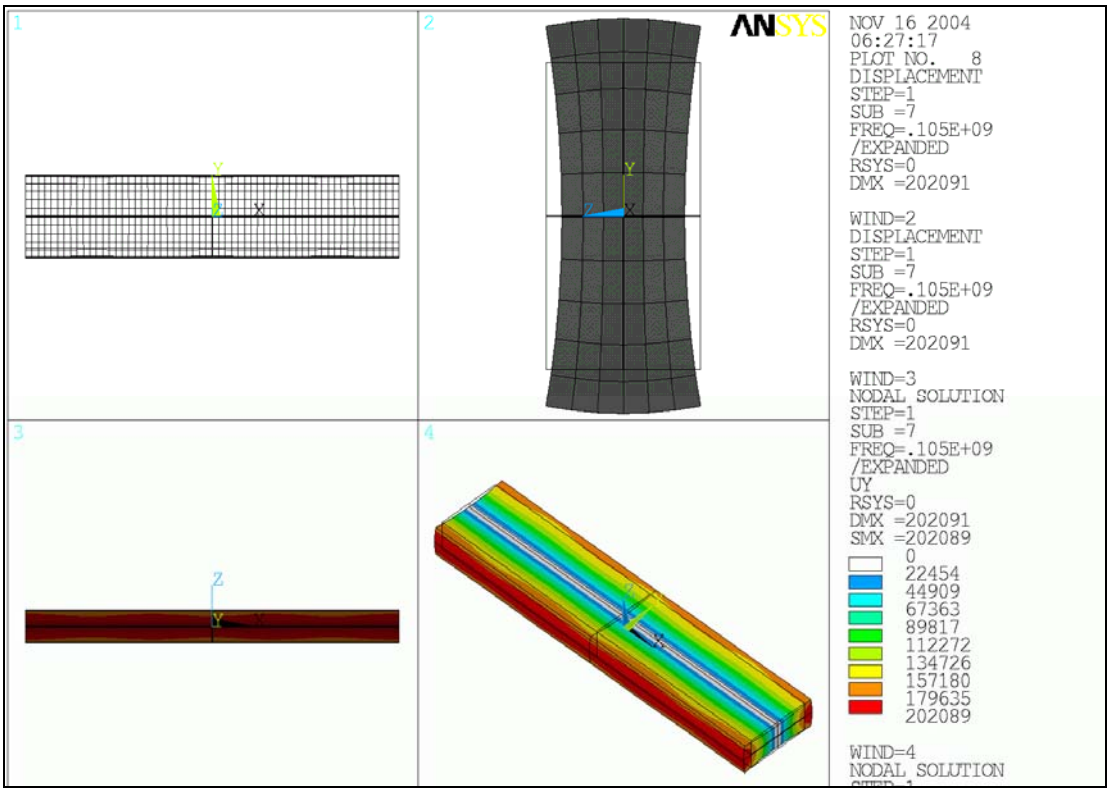


Figure 3.1: ANSYS simulations of a 105MHz SiBAR

3.3 IBAR

Process variation that results in frequency shift has been a major issue in large-scale mass production of MEMS resonator. However, through clever resonator design where the stiffness and mass of the resonator change at the same rate, the resonant frequency can be kept constant even under the presence of process variation.

The I-shaped bulk acoustic resonator (IBAR) is an extensional mode resonator with an enlarged flexural electrode for greater electrostatic tunability and reduced motional impedance [7, 8]. Thus, the IBAR is unique in combining high Q with the tunability of flexural resonators. ANSYS simulations of the mode shapes of 6MHz, 12MHz, and 15MHz IBARs are shown in Figures 3.2, 3.3, and 3.4. The ANSYS simulations are provided by Gavin Ho.

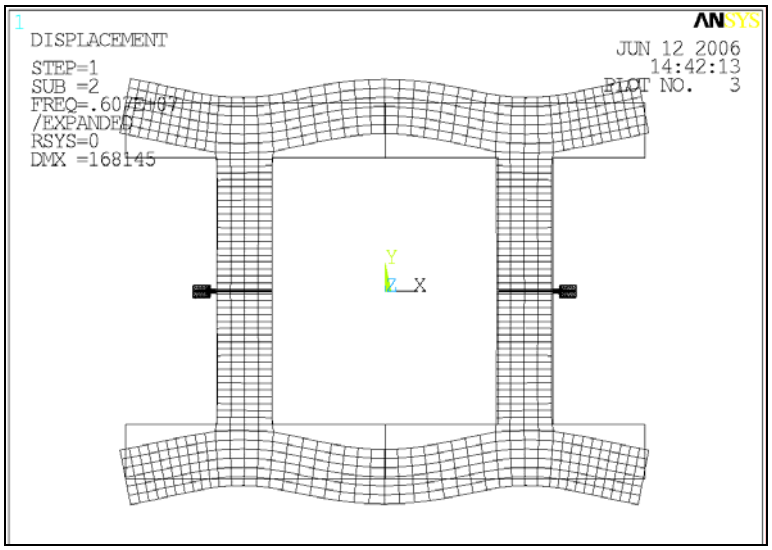


Figure 3.2: ANSYS simulation of a 6MHz IBAR

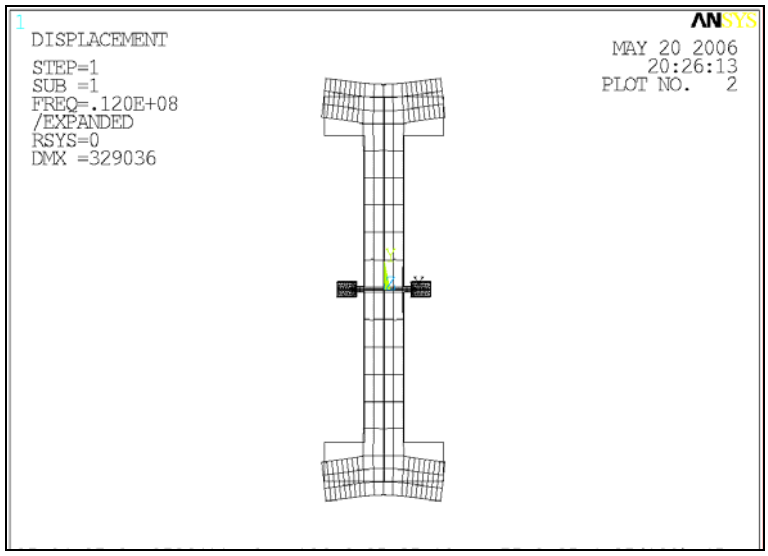


Figure 3.3: ANSYS simulation of a 12MHz IBAR

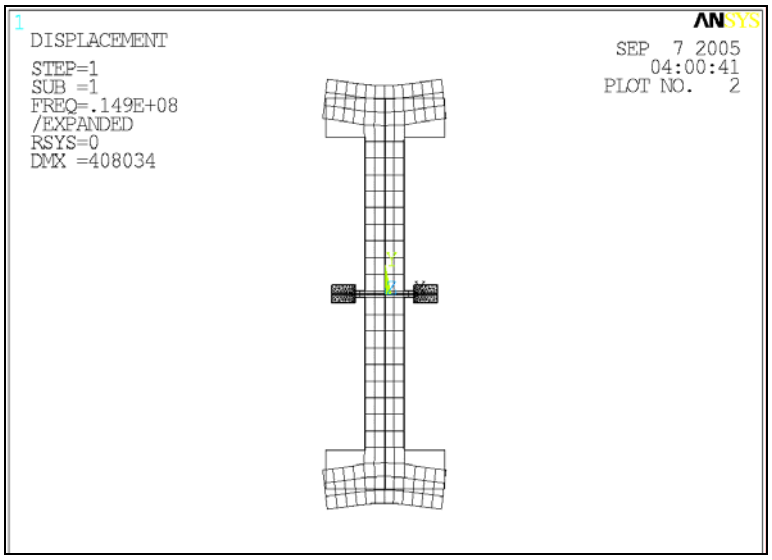


Figure 3.4: ANSYS simulation of a 15MHz IBAR

CHAPTER 4

NANOLITHOGRAPHY

4.1 Introduction to Electron Beam Lithography system and its operating principle

Electron Beam Lithography system is ideal for patterning small area devices with nanometer resolution. The work developed here was done by JEOL JBX-9300FS Electron Beam Lithography (EBL) system. In this EBL system, the beam spot size can be varied from 4nm to 200nm, depending on the acceleration voltage and beam current. The EBL system uses a thermal field emission type cathode and ZrO/w for the emitter to generate an electron beam. The beam generated from the emitter is processed through a four-stage e-beam focusing lens system and forms a spot beam on the work piece.

Pattern writing is carried out on a work piece, which has been coated with an electron beam sensitive resist, by scanning the electron beam. The EBL system adopts a vector scanning and step-and-repeat writing method. It has a two-stage electrostatic deflection system. The position-deflection system (main deflection system) scans over a 500um x 500um area, and it controls precise positioning of the beam. The scanning-deflection system (subsidiary deflection system) scans over a 4um x 4um area, and it performs high-speed beam scanning.

The electron beam generated is accelerated through a 100kV (or 50kV) electrode, and the beam is turned on or off by a blanking electrode when the stage moves. The EBL system is also equipped with electrodes that correct the field curvature and astigmatism due to beam deflection. A detail electro-optical schematic of the EBL system is given in Figure 4.1 [9]

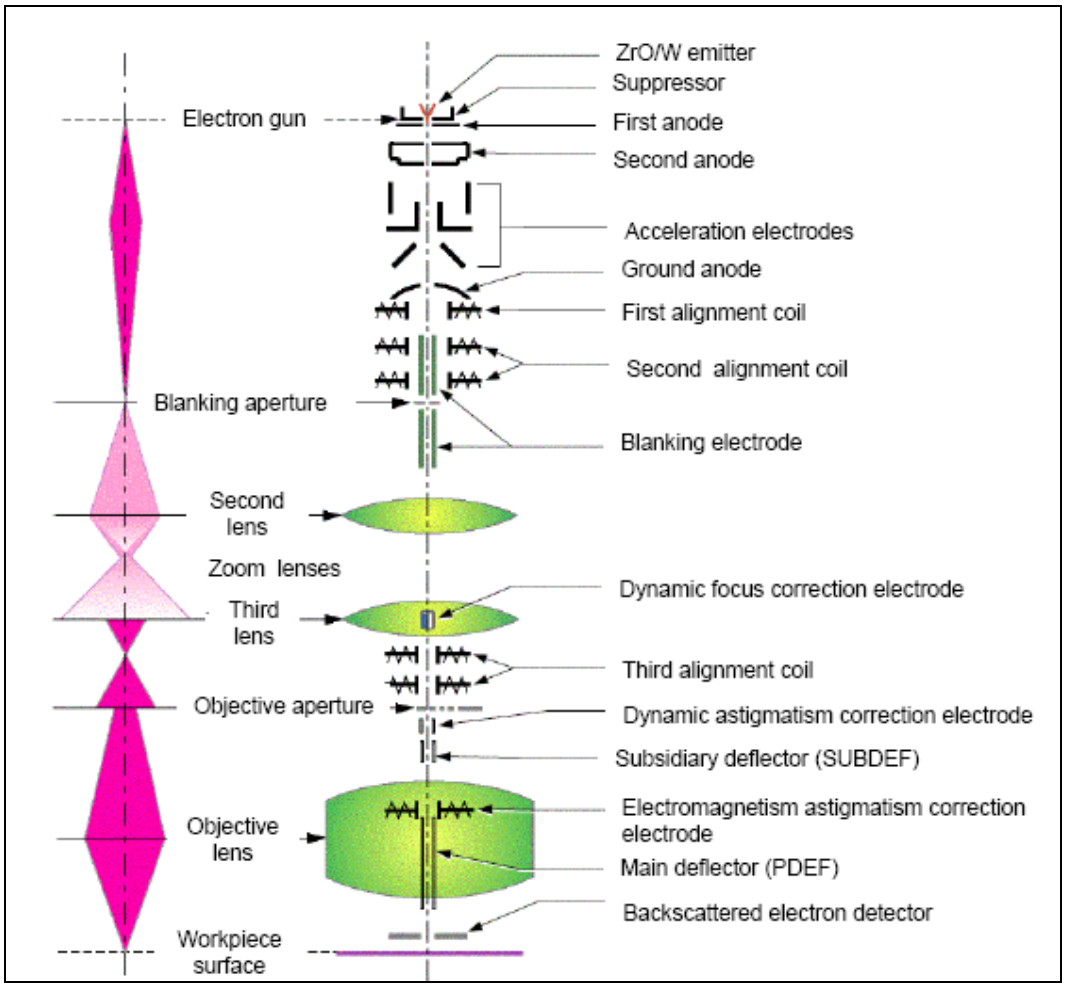


Figure 4.1: Electro-optical schematic of EBL system

The minimum feature that can be resolved by the EBL system depends on several factors, such as the type of resist, resist thickness, exposure dosage, the beam current level, proximity correction, development process, and etching resistance of the particular electron beam resist used. Each of these topics will be discussed in the following sections.

4.2 General procedure

The feature patterned on the electron beam resist can be transferred to the substrate using two methods: the lift-off process or the direct etching process. In a lift-off process, the resist is first spun onto the wafer, exposed by E-beam lithography, and developed in a solution. Next, a masking material, such as Titanium, is sputtered onto the wafer. The wafer is then placed in a resist stripper to remove the resist. The metal that is sputtered directly on top of the substrate where there is no resist will stay, but the metal that is sputtered on top of the resist will be lifted off along with the resist, hence, it is called the lift-off process. The metal left behind becomes the etching mask for the substrate. The negative resist is typically preferred for the lift-off process because it has a slightly angled sidewall profile.

In a direct etching process, a masking material such as silicon dioxide is first deposited onto the silicon substrate. Silicon dioxide is used as a mask because it has high selectivity in silicon etching (1:100). The resist is then spun onto the wafer, exposed and developed. Next, the pattern is transferred onto the oxide mask by reactive ion etching (RIE) or inductively coupled plasma (ICP). One thing to take into consideration is that the electron beam resist will also be etched during the oxide etching. Therefore, the selectivity of the resist to oxide during the etching process will determine the minimum required resist thickness for a given oxide thickness. Figure 4.2 below illustrates both processes.

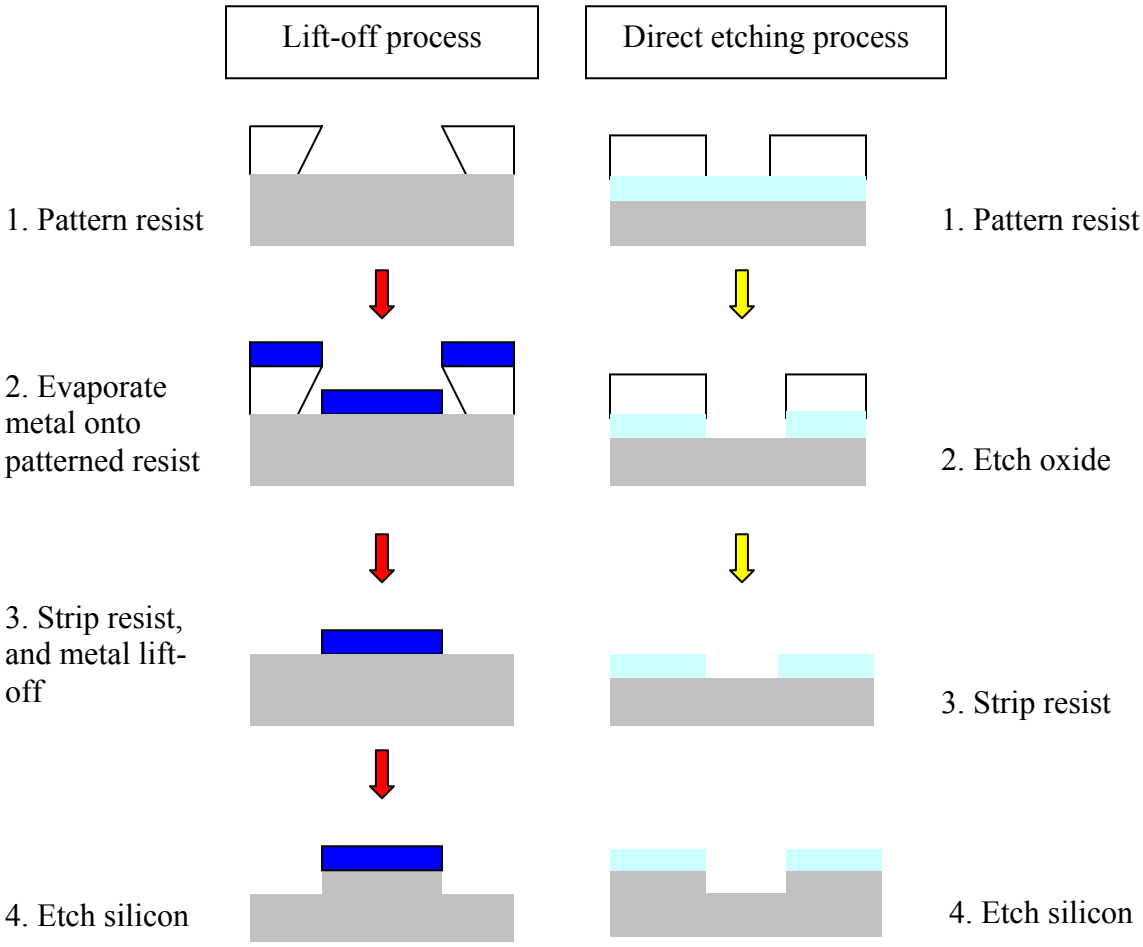


Figure 4.2: Comparison of lift-off process and direct etching process

4.3 Criteria for choosing electron beam resist

The main criteria for choosing the appropriate resist depend on the minimum resolution, sensitivity (hence, exposure time and throughput), and resistance against plasma etching. However, the etching resistance of the resist is not as critical in the lift-off process, since metal is used as the final mask. There are two types of resist: positive-tone and negative-tone. In a positive-tone resist, the area exposed under the electron beam will be removed after development, and the unexposed area will remain. On the other hand, in a negative-tone resist, the area exposed under the electron beam will

remain after development. An extra post-bake step is also required to activate the cross-linking process in the negative resist. Figure 4.3 illustrates the difference between positive and negative resist after exposure and development.

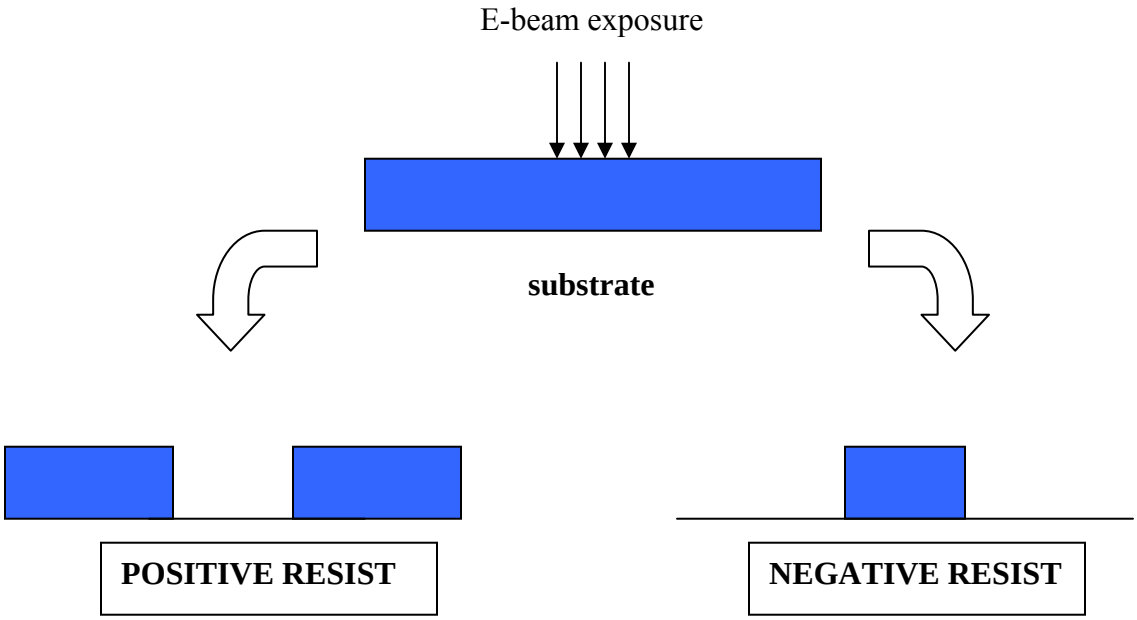


Figure 4.3: Difference between positive and negative resist after exposure and development

Currently, the available positive resists are ZEP520A and PMMA, and the negative resists are HSQ and ma-N. Table 4.1 summarizes the major properties of these resists.

Table 4.1 Properties of commonly used electron beam resist

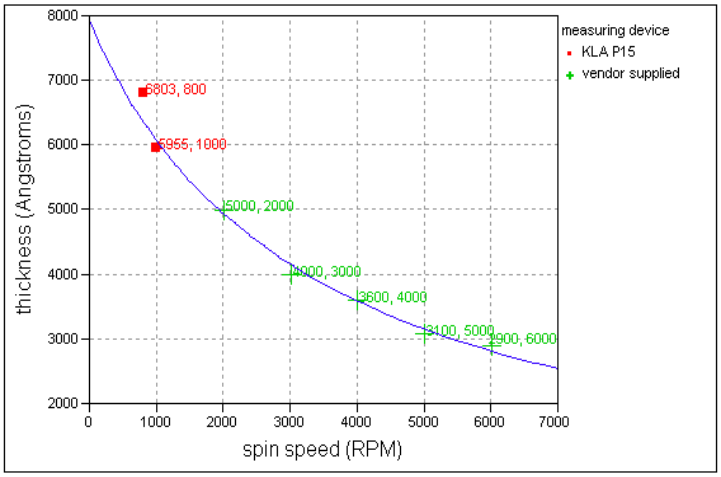
	Tone	Resolution (nm)	Sensitivity (uC/cm^2)	Etching Resistance	Comments
ZEP	Positive	10	200	Good	Expensive, long shelf-life
PMMA	Positive	5	400-500	Fair	Good for lift-off process. Can also be used in deep UV and x-ray lithography
HSQ	Negative	6.5	1000-1200	Good	Exposed resist form SiO_2-like film
ma-N	Negative	<100	400	N/A	Poor adhesion to substrate

In this work, ZEP520A was chosen because it offered the best resolution with the highest etching resistance. The standard procedure for patterning with ZEP resist is given in Table 4.2

Table 4.2 Standard procedure for patterning with ZEP resists

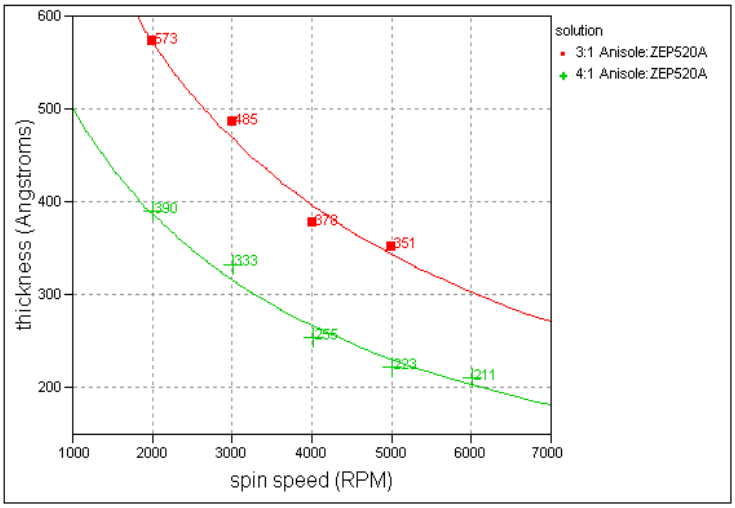
1	Determine the required resist thickness and use the thickness vs. spin-speed curve. For 500nm thick resist, use pure ZEP520A at 2000rpm for 60 seconds. For 50nm thick resist, use 3:1 dilution at 2700rpm for 60 seconds.
2	Use a pipette to take out a few mL of ZEP520A resist and drop them carefully over the wafer
3	Spin the ZEP520A resist on wafer
4	Post-bake at 180C for 2 minutes
5	Expose in Electron Beam Lithography
6	Develop in ZED-N50 for 1.5 minute (variable) and 1 minute in IPA

The ZEP520A thickness vs. spin-speed curves are shown in Figure 4.4 and 4.5. Note that for different range of thickness, different ZEP dilutions are used.



(1/y) = 1.259E-4 + (3.8E-8)x

Figure 4.4 Thickness vs. spin-speed curve for pure ZEP520A



3:1 solution curve fit:
(1/y) = 9.63E-4 + (3.88E-7)x

4:1 solution curve fit:
(1/y) = 1.41E-3 + (5.82E-7)x

Figure 4.5: Thickness vs. spin speed curves for 3:1 and 4:1 dilution of anisole:ZEP520A

The minimum resolution also depends on the resist thickness. Since resist pattern with aspect-ratio greater than 10 is difficult to achieve, so if the resist is too thick, the developed feature may tumble over or not resolved at all. For example, for a 500nm-thick resist, the smallest reproducible width of the pattern is 50nm (AR of 10); to produce a 10nm-wide feature, resist no thicker than a 100nm has to be used. Typically, however, aspect-ratio of 5 or less is preferred and has been shown to be reproducible. On the other hand, if the resist is too thin, there may not be enough resist left after longer cycle of etching. Figure 4.6 shows the maximum resist thickness for various minimum resolutions.

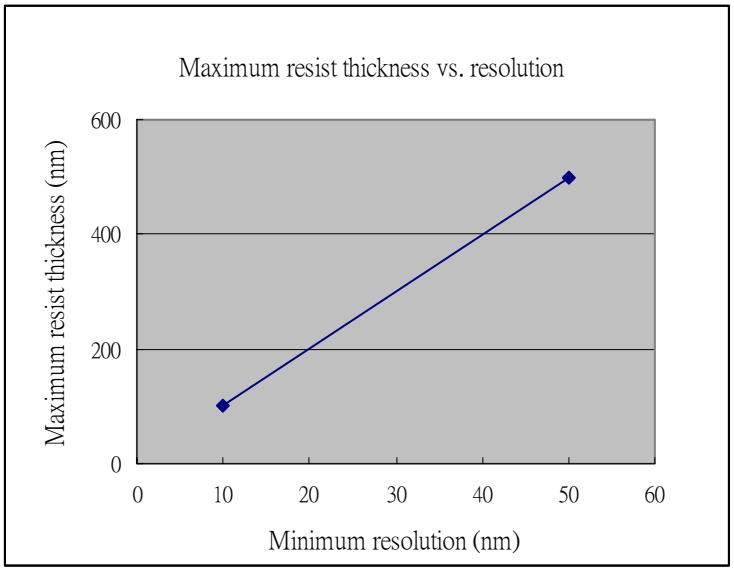


Figure 4.6: Maximum allowable resist thickness for various minimum resolutions

4.4 Trade-off between minimum resolution and exposure time

The minimum resolution is also a function of the beam current. To get a smaller feature size, a lower beam current is required. However, the required beam current decreases exponentially with decreasing minimum feature size. This will limit the maximum throughput because the total exposure time also depends on the beam current. The total exposure time is a function of dose, beam current and total writing area. The equation to estimate the total exposure time is given by:

$$Time = \frac{Dose \times Area \times Fill\_factor}{current}$$

The typical exposure time to resolve a 10nm resolution at 100pA beam current for a $1cm^2$ area with 1% fill-factor is about 5 hours. This becomes impractical when large numbers of chips need to be patterned. One way to resolve this problem is to increase the

beam current at the expense of resolution. Table 4.3shows the beam current required for different minimum feature size.

Table 4.3: Beam current requirement for different minimum feature size

Beam Current	Beam diameter	Minimum resolution
100pA	4nm	10nm
1nA	8nm	20nm
10nA	30nm	60nm

As a comparison, to pattern a $1cm^2$ chip with 1% fill-factor at 2nA versus 100pA is calculated below:

$$\frac{200uC/cm^2 \times 1cm^2 \times 1\%}{2nA} = 15\,\text{min}$$

$$\frac{200uC/cm^2 \times 1cm^2 \times 1\%}{100\,pA} = 5hrs$$

4.5 Proximity effect

During the exposure step, scattering effect from the electron beam causes pattern distortion. The principle behind electron beam lithography is that when the electron strikes the resist, some molecular chains in the resist molecule are broken. The exposed region becomes more dissolvable when placed in a developer solution. The proximity effect occurs when the electron scattering effect leads to undesirable exposure in the resist. There are two types of scattering event, namely forward scattering and backward scattering. Forward scattering leads to broadening of the image and backward scattering produces fog of exposure.

In forward scattering, an incident electron collides with the electron in one of the atoms of the resist. During the collision, some kinetic energy is transferred from the incident electron to the resist molecule and breaks the bond between two adjacent resist molecules. In backward scattering, an incident electron collides with the nucleus of the substrate atom. Since the nucleus is heavier, the scattering event is mostly elastic and results in a large scattering angle. This large angle may cause some electrons to return at a distance significantly far away from the incident beam, and lead to additional exposure in the resist. Together, both the forward scattering and the backward scattering broaden the exposure area and limit the resolution.

Forward scattering can be minimized by using a thinner resist and applying a higher accelerating voltage. Backward scattering can be minimized, where possible, by choosing a substrate with smaller atomic mass unit.

Commercial software exists that can produce a dose-corrected fractured data file for proximity correction. The correction software calculates the concentration of surrounding features, suitably weighted by their distance from the area to be exposed, and subtracts the amount of backward scattered exposure that one expects to see. It then modifies the exposure time (hence, dose) per pixel to compensate for the proximity effect. Without the use of proximity correction software, the smallest features cannot be resolved reliably.

To study the proximity effect, a thin layer of resist (50nm) was used in a test. As a comparison, one sample was patterned with the optimal dosage calculated by the proximity correction software, and the other sample was patterned without proximity correction. Results have shown that from the same drawing, the highest resolution

without proximity correction was 50nm, but after proximity correction, the resolution improved to 23nm. Figure 4.7 are SEM images demonstrating the effect of proximity correction on minimum resolution.

50nm (without proximity correction) 23nm (with proximity correction)

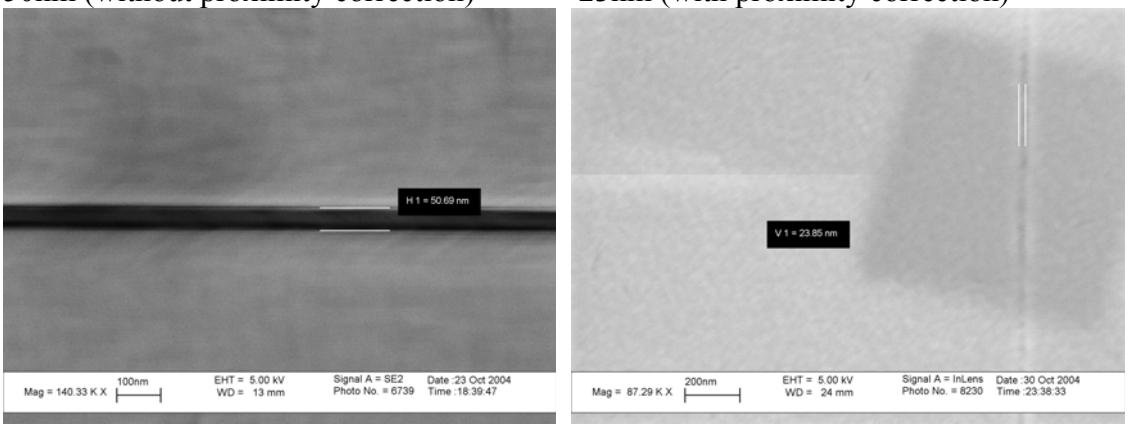


Figure 4.7: Effect of proximity correction on minimum resolution

4.6 Dose dependency and shot modulation

The optimal dose for any particular pattern is a function of many variables, including the pattern size, the pattern density, the resist thickness, the accelerating voltage, and the substrate atomic mass unit [11]. It is difficult to model all of these variables at the same time because the effect of each parameter is difficult to control. Nevertheless, there are some general observable trends that one can use to predict the optimal dose.

In general, larger pattern size requires fewer doses because the proximity effect becomes more significant in a larger exposed area. In the same way, as the density of the pattern increases, the required dose also decreases because as the area to be exposed are getting closer, the proximity effect causes nearby area to be exposed.

The second thing to consider is the resist thickness. As mentioned earlier, the principle behind electron beam lithography is that when an accelerated electron strikes a resist molecule, the bond between two adjacent resist molecules is broken. This bond-breaking event occurs multiple times as the electron accelerates down its path and collides with many resist molecules. When sufficient bonds are broken, the exposed region becomes more dissolvable in the developer. However, as the resist thickness decreases below about a 100nm, there is less distance for the electron to travel and collide with the resist molecule. Hence, a higher dose is required to break the same number of molecular bonds.

Accelerating voltage also plays an important role. For the same reason that higher accelerating voltage results in a smaller beam spot, and therefore smaller feature size, the minimum required dosage increases with higher accelerating voltage. This is because the increasing accelerating voltage results in a smaller number of scattering events, and thus a higher does is needed.

Lastly, the substrate atomic mass unit, or the atomic size of the substrate, will also affect the minimum required dose. As discussed previously, backscattering event occurs when an electron strikes the nucleus of the substrate atom and bounces back into the resist. If the size of the substrate atom is small, the chances of an electron passing through two substrate atoms without hitting the nucleus become large, and less backscattering event will occur. On the other hand, if the size of the substrate atom is large, more backscattering event is likely to take place. Typically, however, the substrate material is determined by the type of the application, so it cannot be changed randomly. Table 4.4 summarizes the dose dependency of various factors.

Table 4.4 Summary of dose dependency due to various factors

	Increase/Decrease	Required dose
Pattern size	↑	↓
Pattern density	↑	↓
Resist thickness	↓	↑
Accelerating voltage	↑	↑
Substrate atomic mass unit	↑	↓

When one tries to characterize the optimal dosage, one can use the shot modulation function in the EBL system to determine the best dosage for a particular design and resist thickness.

An example of using shot modulation to optimize the required dose for a particular design is provided later in this chapter. One can also refer to the job deck file and schedule file in the appendix section for more detail information.

4.7 Shot pitch, field stitching correction and calibration

Shot pitch is the minimum distance between two adjacent spots to be exposed. During the beam scanning, the EBL system has a minimum dwell time over each spot, which is determined by the beam blanking frequency and the scanning speed of the main deflector. For a particular dose, the shot pitch needs to be large enough so that the minimum time spent at a point will not exceed the dosage allowed for that point.

Since the maximum scanning field is 500um x 500um, for any pattern larger than the maximum scanning field, the stage has to move mechanically and the laser positioning system is utilized to measure the exact position of the stage. Field stitching error occurs when individual 500um x 500um field is not perfectly align to the adjacent

field. Figure 4.8 shows an example of field stitching error, where two isolated pads are connected together.

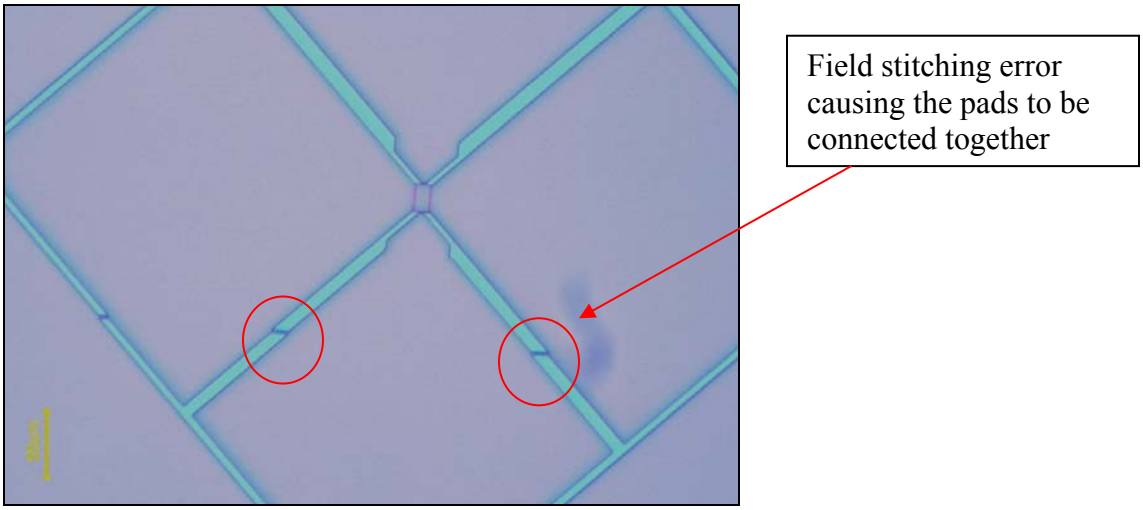


Figure 4.8: Example of field stitching error

In order to obtain the minimum feature resolvable by the EBL system and correct any error such as field stitching, a series of calibration needs to be performed at the beginning of each exposure job. Calibration of the EBL system is based on determining the mark position on the stage and the beam spot size by controlling the work stage position with the laser-interferometer positioning system. Some of the most critical and commonly used calibrations are described here.

CURRNT detects the beam current with a Faraday cup that has pico-ampere resolution. The optimum scanning speed of the electron beam in pattern writing is determined on the basis of the beam current measured.

INITBE determines the position of the backscattered electron marks on the stage and corrects beam position error.

PDEFBE determines the height-correction coefficients for the main deflection when the focus is kept unchanged. It corrects the amplitude and rotation of the main deflection field (500um x 500um).

SUBDEFBE determines the height-correction coefficients for the subsidiary deflection when the focus is kept unchanged. It corrects the amplitude and rotation of the subsidiary deflection field (4um x 4um). PDEFBE and SUBDEFBE are used together to correct field stitching error.

DISTBE measures and corrects the distortion in deflection within the field.

SFOCUS performs astigmatism correction and sets the focus.

AE (absorbed electron) detection calibrates beam position and stage position based on physical location of the mark on stage. It also calculates the beam spot size.

HEIMAP measures the height variation in a specified area across the wafer and takes the average height for the focus value on the work piece.

For more detail information and explanation on how to set up proper calibration, one can refer to the JEOL JBX-9300FS General Statements manual [12].

4.8 Define minimum feature using the EBL system

In order to determine the minimum resolvable feature for a particular resist thickness and beam current level, a test pattern was drawn with increasing width from 10nm, 20nm, 30nm, 40nm, 50nm, 60nm, 70nm, 80nm, 90nm, 100nm, 200nm, 300nm, 400nm, 500nm, to 1um. The SEM picture below shows the test pattern. All the features were patterned using ZEP resist with 210uC/cm^2 base dose. Figure 4.9 shows the test pattern on silicon substrate.

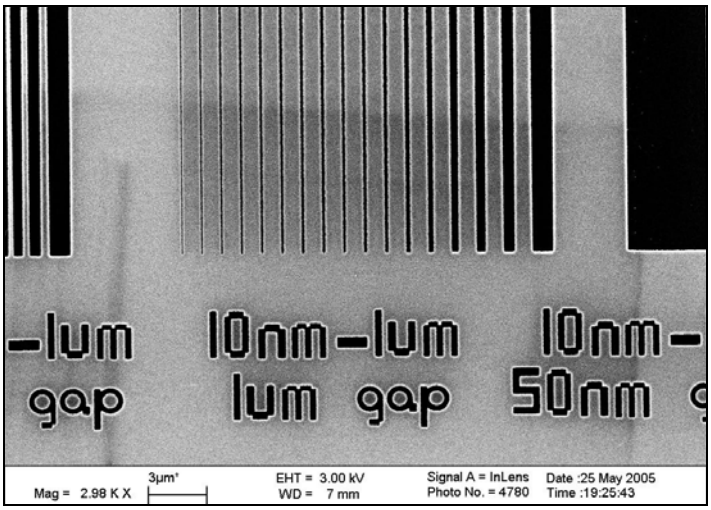


Figure 4.9: Test pattern for characterizing minimum feature size

Figure 4.10 are SEM images showing minimum feature patterned using 50nm-thick ZEP resist on silicon substrate at 2nA. The minimum resolvable feature is 28nm.

Patterned lines

28nm minimum feature

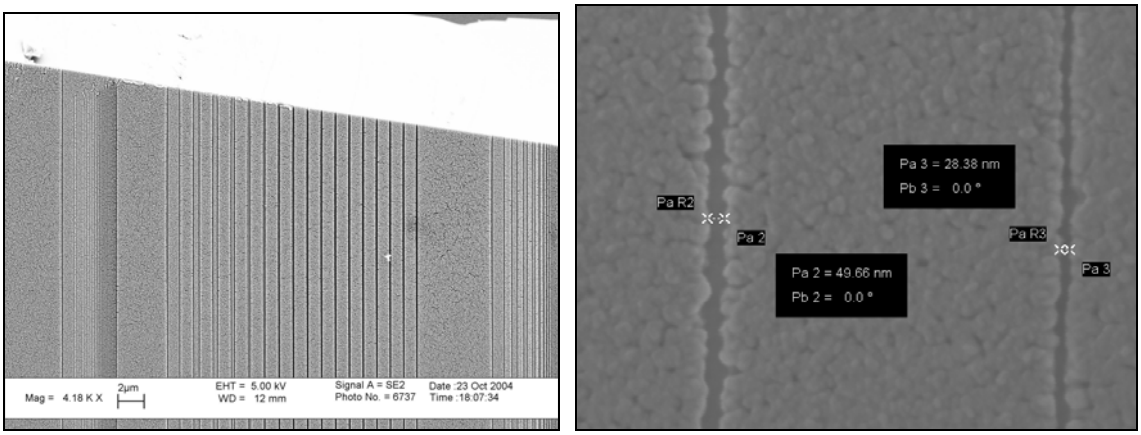
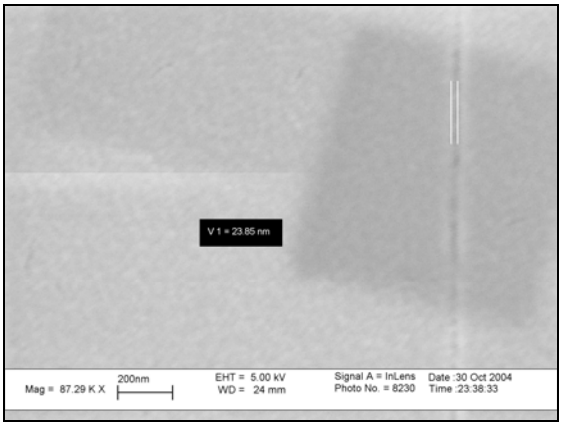


Figure 4.10 Minimum feature pattern using 50nm-thick ZEP resist at 2nA

Figure 4.11 show SEM images of feature patterned using 50nm-thick ZEP resist on 60nm-thick oxide on silicon substrate at 2nA. The minimum feature prior to oxide etching was 23nm, while the minimum feature after oxide etching was 50nm.

Before oxide etching, 23nm



After oxide etching, 50nm

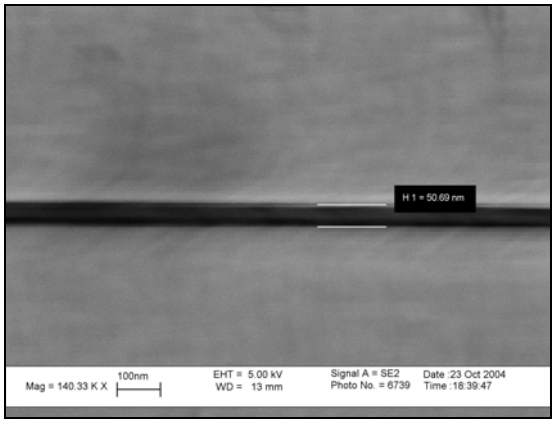


Figure 4.11 Minimum feature pattern using 50nm-thick ZEP resist on 60nm-thick oxide at 2nA

4.9 Example of patterning periodic structure with various spacing

In many applications such as photonic grating or coupler, periodic structures are used to create certain optical properties. In these applications, it is not sufficient to pattern only small feature, but it is also necessary to pattern repeatable structure with exact dimension. However, variations often exist during the process of exposure, development, or etching of the final structure. Therefore, some techniques have been developed to compensate for these unknown effects. Here, an optical grating structure is used as an illustration. The structure is composed of a series of 160nm-wide beam, separated by 105nm and 355nm spacing on either side. Similar example where circles were used as the periodic structure can also be found, as described by Yamashita [13].

The first approach is to design and draw a series of periodic structure where the beam width and the gap spacing have slightly offset. Figure 4.12 shows four different designs.

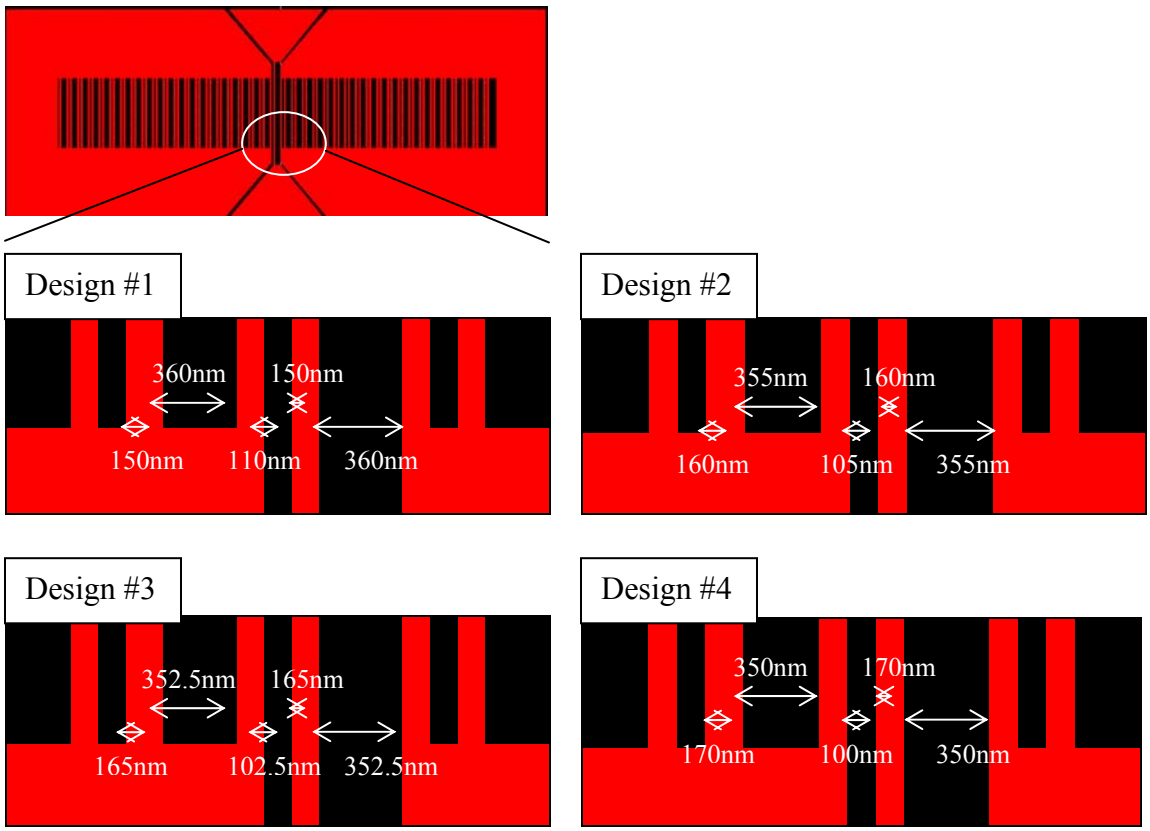


Figure 4.12: Four design layout of optical grating structure

Next, the same structure is put on different layers (data type) for shot modulation. One can experiment with different exposure dosage to find out which dosage and design give the final pattern that is closest to the target dimension. Figure 4.13 shows grating structure with four different designs on nine different layers for shot modulation.

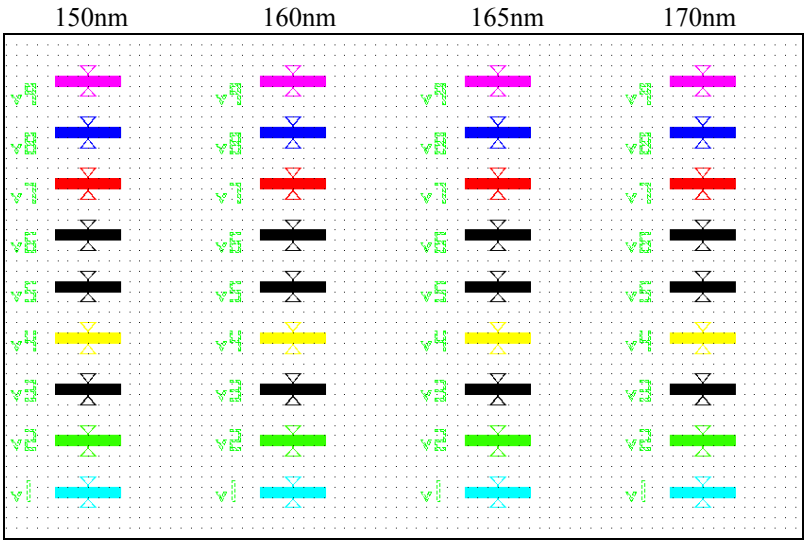
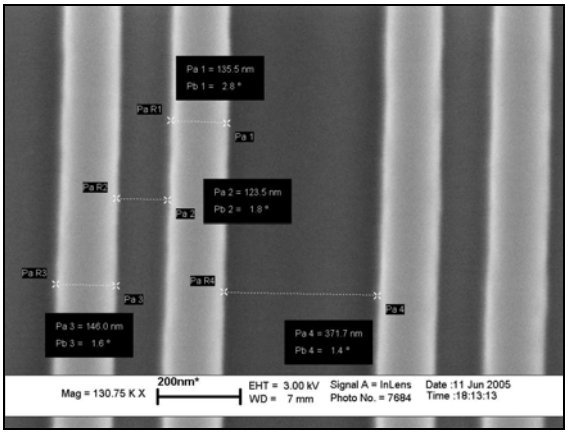


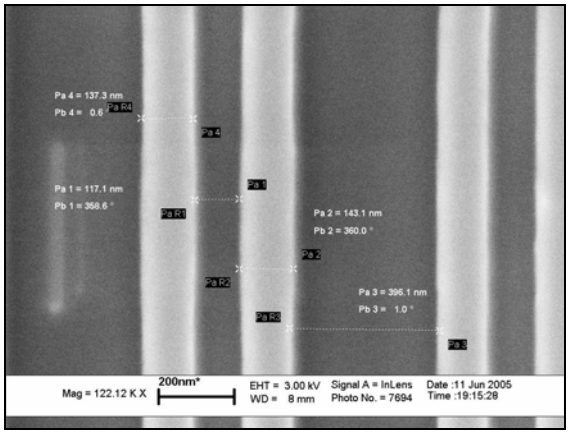
Figure 4.13: Design layout of optical grating structure with shot modulation.

The grating structure was patterned on a sample with 120nm-thick ZEP resist on 90nm-thick oxide on silicon substrate. The following SEM images show the line width measurement after E-beam exposure and development.

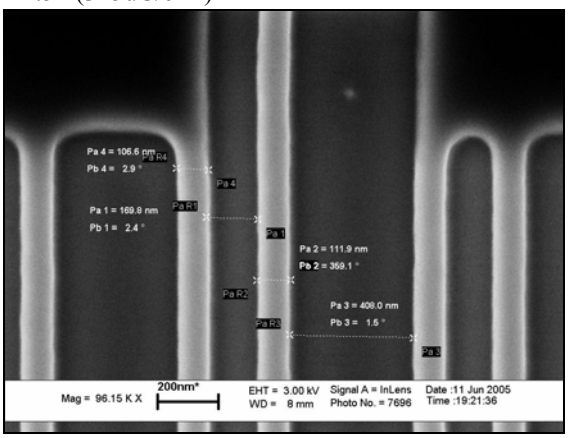
1x (210uC/cm^2)



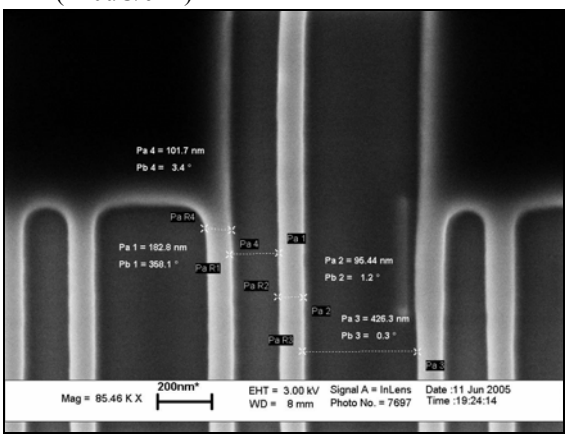
1.25x (260uC/cm^2)



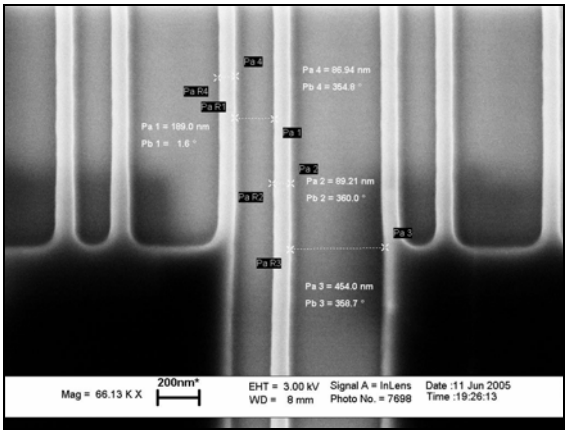
1.5x (315uC/cm^2)



2x (420uC/cm^2)



2.5x (525uC/cm^2)



3x (630uC/cm^2)

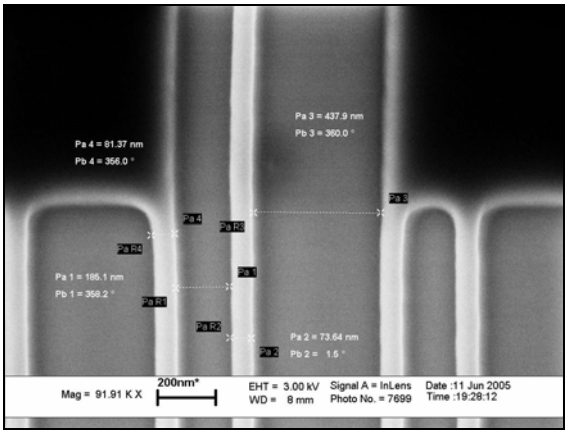


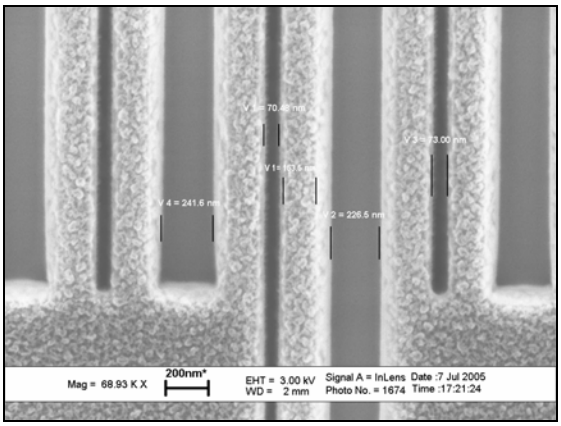
Table 4.5 summarizes the line width measurement from design #2 at various shot modulation.

Table 4.5 Summary of line width spacing after E-beam patterning

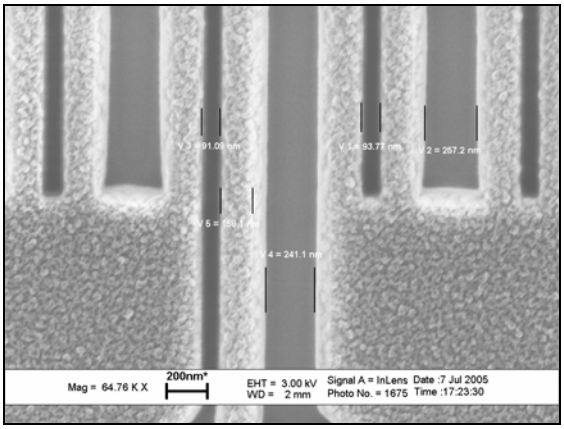
Base dose modulation	Dose modulation (uC/cm2)	Spacing 1 (nm)	Beam width (nm)	Spacing 2 (nm)
1x	210	372	135.5	123.5
1.25x	260	396	143	117
1.5x	315	408	112	170
2x	420	426	95	183
2.5x	525	454	89	189
3x	630	438	73.5	185
Target dimension		**355**	**160**	**105**

In the next step, the oxide on the sample was etched, and the line width of the grating structure was measured again. The following SEM pictures show the measurement results.

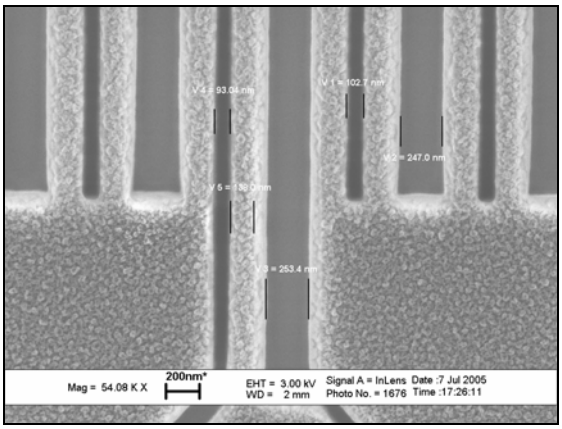
1x (210uC/cm^2)



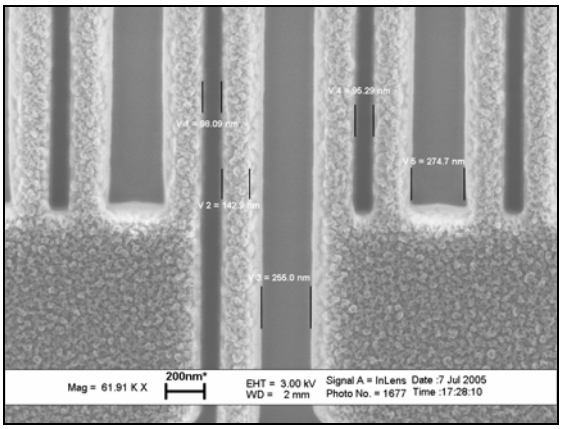
1.25x (260uC/cm^2)



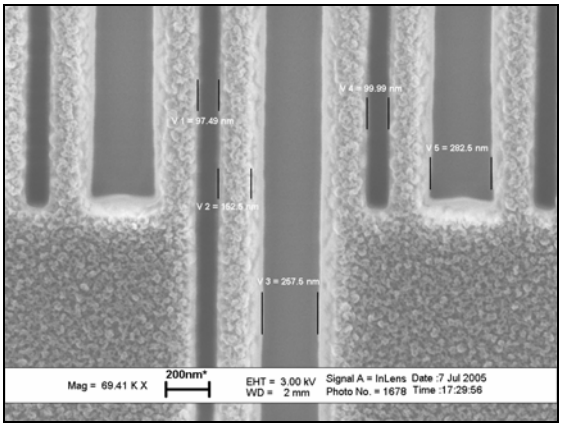
1.5x (315uC/cm^2)



2x (420uC/cm^2)



2.5x (525uC/cm^2)



3x (630uC/cm^2)

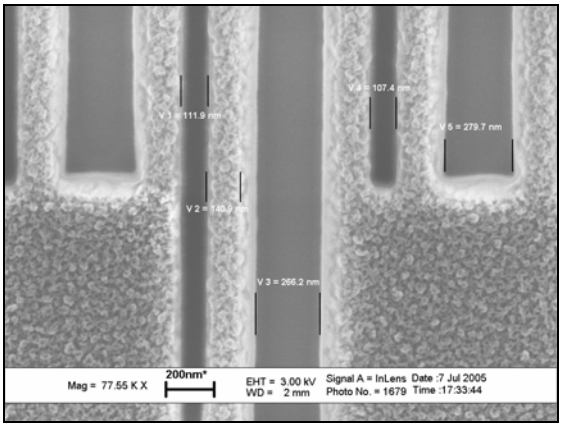


Table 4.6 summarizes the line width measurement of the grating structure after the oxide is etched.

Table 4.6 Summary of line width spacing after oxide etching

Base dose modulation	Dose modulation (uC/cm2)	Spacing 1 (nm)	Beam width (nm)	Spacing 2 (nm)
1x	210	226.5	163.5	70.5
1.25x	260	241	159	91
1.5x	315	253	138	93
2x	420	255	143	98
2.5x	525	257.5	152.5	97.5
3x	630	266	141	112
Target dimension		**355**	**160**	**105**

One can see that the line width measurement of the grating structure differed significantly before and after oxide etching. This was because the profile of the oxide etching was slightly angled and not perfectly straight. Therefore, several designs were necessary to determine the one that yields the final dimension closest to the target dimension. Figure 4.14 shows SEM images of the final grating structure etched in silicon within close range (+/- 5 nm) of the target dimension.

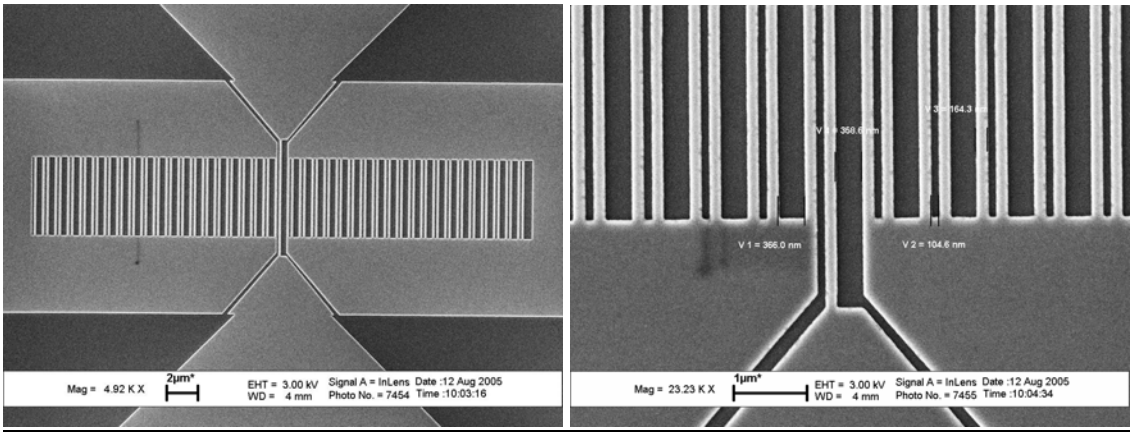


Figure 4.14: Final grating structure etched in silicon (164.3nm-wide bean with 104.6nm and 358.9nm spacing)

One can also fine-tune the pattern by varying the development time. Experiments have shown that when the development time increased from 1 minutes and 30 seconds to 2 minutes, the exposed region was broadened by about 5-10 nm.

4.10 Metrology and thickness measurement

The metrology equipments used in this work include Nanospec Refractometer, Tencor Profilometer, and LEO SEM/EDS. Nanospec Refractometer can measure the film thickness, given the Cauchy coefficient of the material. The selectivity and etch rate can be determined by measuring the film thickness (ZEP resist, oxide, or silicon) before and after etching. The Cauchy coefficient of the ZEP resist is given below [14]:

$$n = n_o + \frac{n_1}{\lambda^2} + \frac{n_2}{\lambda^4}$$

$$n_0 = 1.541093$$
$$n_1 = 4.113002 \times 10^5$$
$$n_2 = 4.070357 \times 10^{12}$$

Absorption coefficient = 0, Unit of λ: (Å)

The Tencor Profilometer can measure the surface roughness and physical depth of an etched trench. Since it measures the surface profile physically, it can be used to verify the measurement from the Nanospec Refractometer when the optical fit is poor. However, the curvature of the stylus tip is 2 um, so any trench opening less than 2um cannot be measured accurately.

High-resolution SEM has been used extensively to view the cross-section of sub-micron feature. One can also use the EDS (energy dispersive spectrometry) installed on

the SEM to analyze the chemical composition of a particular point of interest on the sample. The EDS is capable of picking up any element greater than fluorine, and this is especially helpful when identifying unknown residue deposited on the sample. Figure 4.15 shows the EDS spectrum of a sample where the only element detected is silicon.

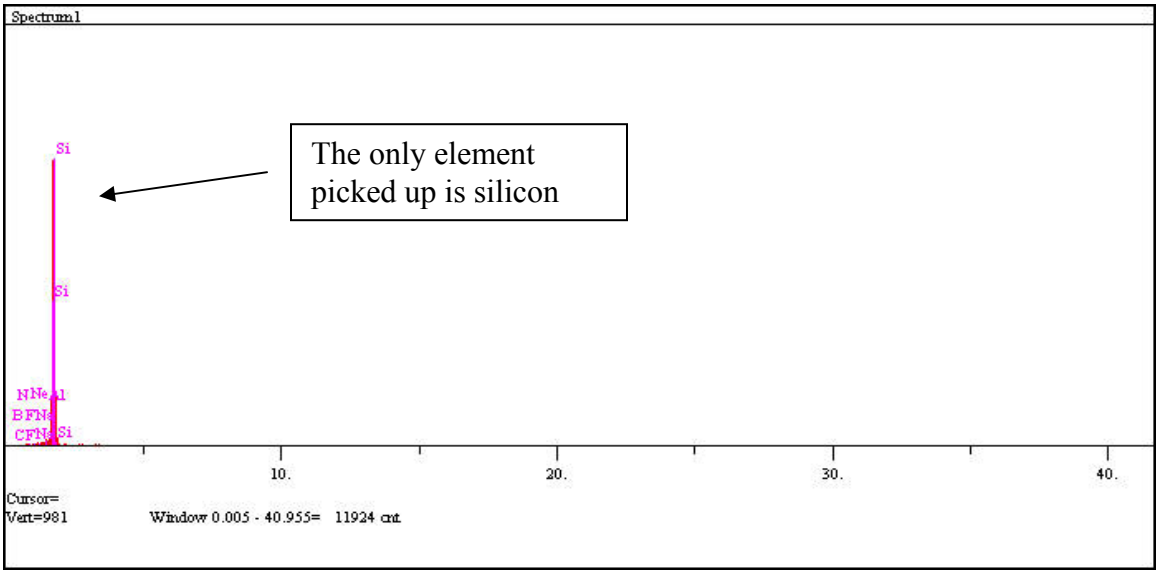


Figure 4.15 Energy dispersive spectrum of a sample

4.11 Sample cleaning and residual removal method

Dust particles in the air or from human source can easily fall on the wafer surface during wafer handling. This will not only leave spot on the sample, but also introduce non-uniformity in the resist when the resist is spun on the wafer. Therefore, one should minimize the time between the wafer is taken out of the storage box and when the resist is spun on the wafer. In addition, when the ZEP resist is exposed to air, it will pick up the moisture in the air and bubbles will form inside the resist. These bubbles will create streaks when the resist is spun on the wafer. Secondly, the shelf life of ZEP is about 6

months and the quality of the ZEP degrades over time. Therefore, one has to pay attention not to use expired ZEP.

There are several cleaning methods to remove photoresist or other organic materials on the wafer prior to E-beam patterning. Organic contaminant can be removed by placing the wafer in H_2SO_4 mixed with H_2O_2 at 120^oC (piranha clean). Next, one can clean the sample with oxygen plasma in the RIE for 10-20 minutes, or use the Gasonic Asher to do oxygen plasma clean at elevated temperature for 2 minutes. This will remove any residue left on the wafer.

During the etching step, residue may form inside the chamber due to a particular etching chemistry. This residue may transfer undesirable pattern to the substrate. This has been a major concern, especially when one tries to etch the electrode gap in a resonator device. Since any small residue deposited inside the electrode gap will short the resonator device and annul the device operation, an oxygen plasma cleaning step is typically added after each etching step to eliminate residue formation. Figure 4.16 shows a SEM image of residue deposited inside the electrode gap.

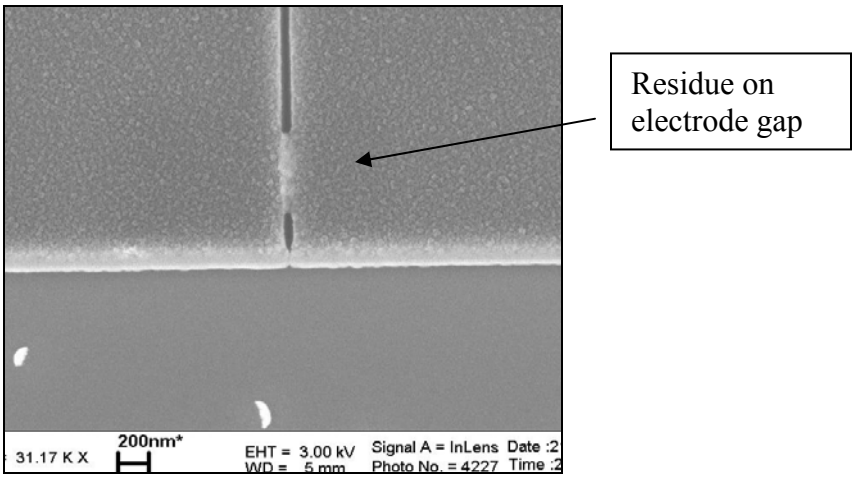
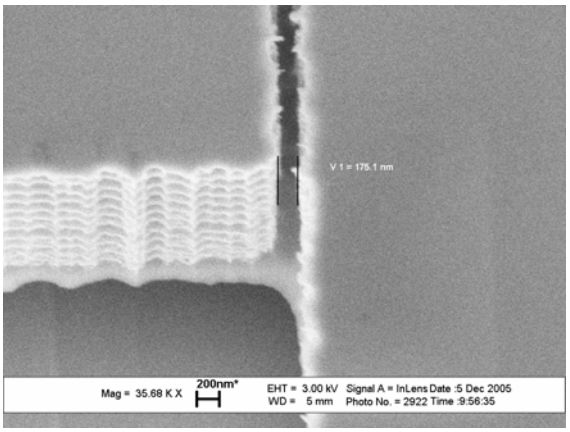


Figure 4.16: SEM image of residue deposited inside the electrode gap during etching.

Figure 4.17 shows SEM images of a sample before and after the oxygen plasma clean.

Before O2 clean



After O2 clean

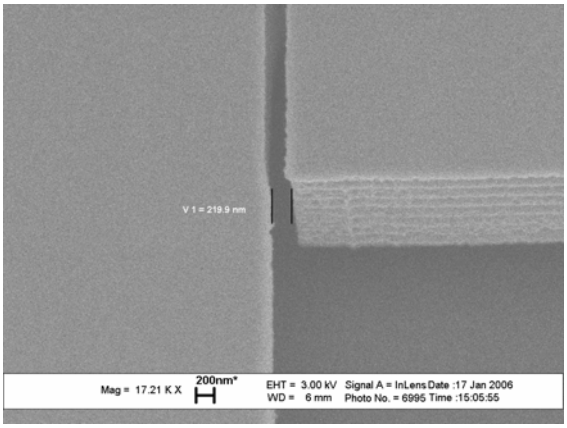


Figure 4.17: SEM image of sample before and after oxygen plasma clean

CHAPTER 5

PLASMA ETCHING

5.1 Etching resistance and selectivity of ZEP resist

Since most electron beam resist does not provide sufficient resistance against silicon etching, an oxide mask is needed for etching deep trench in silicon. Therefore, one needs to consider the selectivity of the resist to oxide in the etching process. Among all the available electron beam resist (positive-tone), the ZEP resist offers the highest etching resistance. HSQ also has high etching resistance, but it is negative-tone. Typical selectivity of ZEP resist to oxide in plasma etching is less than 1:2. Table 5.1 lists the process flow for etching oxide and silicon.

Table 5.1 Process flow for etching oxide and silicon

1	Determine the minimum feature size. Example: 50nm resolution
2	Determine the maximum resist thickness with aspect ratio less than 10. Choose resist thickness to be 300nm.
3	Based on the selectivity of ZEP resist to silicon (1:1), determine the maximum depth that can be etched in silicon. In this case, 300nm-thick resist can guarantee at most 300nm-deep trench in silicon.
4	Alternatively, use an oxide mask for etching deeper trench in silicon. The selectivity of oxide to silicon is between 1:20 to 1:50 in standard Bosch process.
5	Deposit 50nm-thick oxide mask for maximum trench depth of 2.5um in silicon.

5.2 Characterization of silicon dioxide etching

As mentioned earlier, the oxide mask thickness is determined by the selectivity of the ZEP to oxide during the etching process. However, the maximum oxide thickness is also limited by the thickest ZEP resist that can be spun on the wafer. Based on the ZEP resist spin-curve, the thickest ZEP resist that can be spun on the wafer is about 0.6um.

Two different oxide recipes have been developed and characterized in this work. The first oxide recipe used CF_4 and H_2 with an oxide etch rate between 200-250A/min. This recipe was mainly developed to etch very thin oxide (~50nm), because it offered very good control over the etch rate, excessive over-etching can be avoided using this recipe. Table 5.2 provides detail information for oxide recipe #1.

Table 5.2 Detail information of oxide recipe #1

Pressure (mTorr)	CF_4 (sccm)	H_2 (sccm)	O_2 (sccm)	RF1/RF2 (W)	Oxide etch rate (A/min)	ZEP etch rate (A/min)	Selectivity ZEP:Oxide
25	25	2	1	100/300	200-250	360	1:1

The sidewall of the trench etched using this recipe had a slightly angled profile. This resulted in smaller gap at the bottom of the oxide trench than the original trench opening. Therefore, one can use this trick to obtain smaller feature (10nm or less) that is beyond the capability of E-beam lithography. Figure 5.1 shows SEM images of the oxide trench profile with 100nm-wide opening at the top and 29nm-wide opening at the bottom.

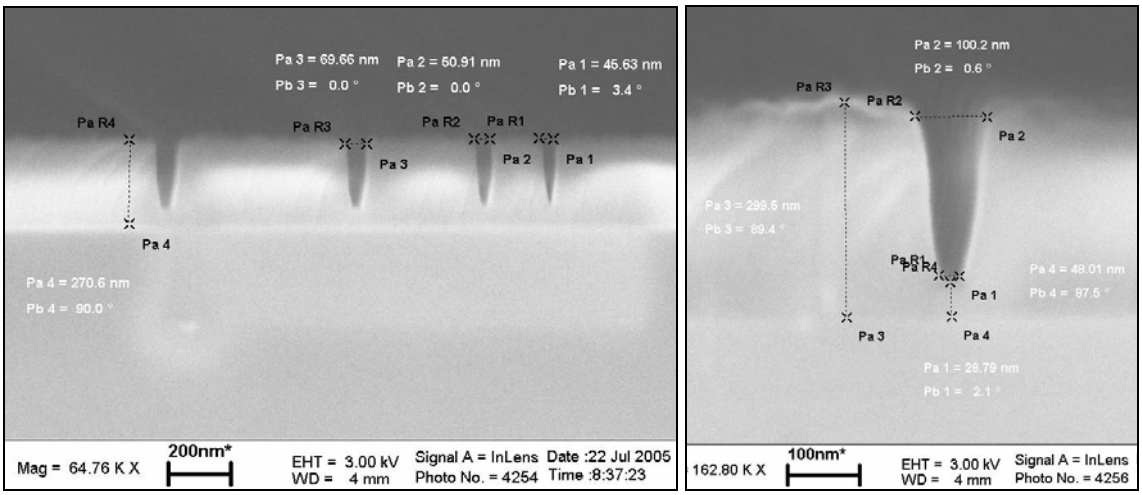


Figure 5.1: SEM image of oxide trench profile with reduced gap at the bottom

In this oxide etching recipe, the selectivity of ZEP resist to oxide can be improved by increasing the H2 concentration. Experiments have shown that the selectivity of ZEP resist to oxide increased from 1:1 at 10% H_2 concentration to 1:1.5 at 20% H_2 concentration.

However, this oxide recipe also created a lot of polymerization inside the chamber. This polymerization will not only contaminate the chamber and reduce the etch rate, but it will deposit a lot of residue on the sample. The residue deposited on the sample can mask the silicon underneath and resulted in pillar after silicon etching. Figure 5.2 shows SEM images of residue deposited on a sample after oxide etching (left) and the silicon pillar formed due to residue masking (right).

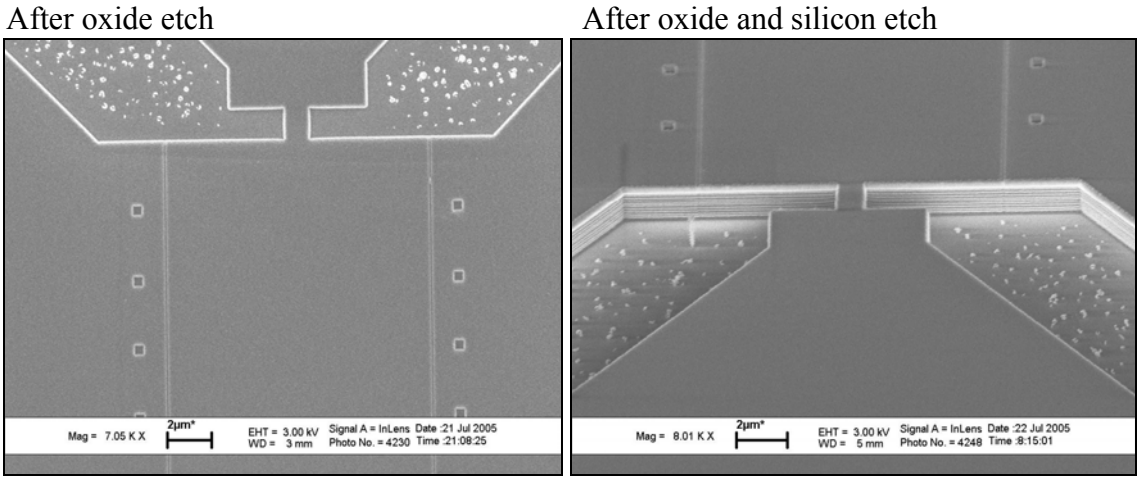


Figure 5.2: SEM images of residue deposited on a sample during oxide etch (left) and formation of silicon pillar due to residue masking (right)

It was shown that the amount of polymerization decreased with lower H_2 concentration. Therefore, the H_2 content was kept under 10%.

The second oxide recipe used CF_4 and C_4F_6 with an oxide etch rate between 1300-1750A/min. This recipe was developed to etch thick oxide because it had a faster etch rate. Table 5.3 provides detail information of oxide recipe #2.

Table 5.3 Detail information of oxide recipe #2

Pressure (mTorr)	CF_4 (sccm)	C_4F_6 (sccm)	O_2 (sccm)	Ar (sccm)	RF1/RF2 (W)	Oxide etch rate (A/min)	ZEP etch rate (A/min)	Selectivity ZEP:ox
5	40	20	3	15	400/250	1300-1750	1460	1:1.2

The second oxide recipe was much cleaner and did not leave any residue after the oxide was etched. This oxide recipe also had an angled sidewall profile, and very small oxide opening was demonstrated. Figure 5.3 shows SEM image of a sample with 12nm-wide oxide opening.

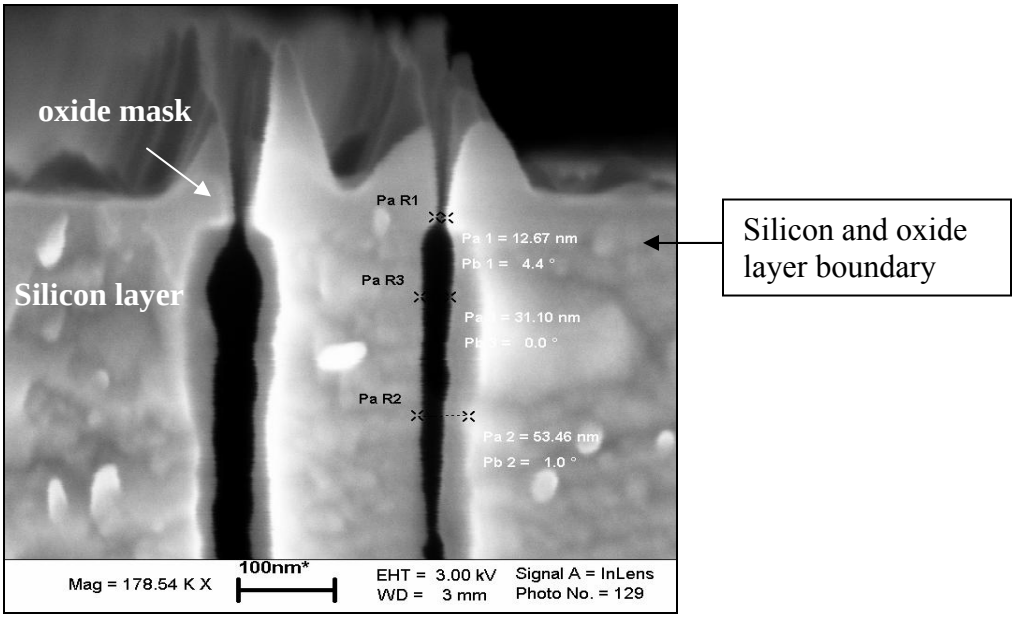


Figure 5.3: SEM image of a sample with 12nm-wide oxide opening.

However, the sidewall profile from this recipe was very rough, so it was harder to control the lateral dimension. Figure 5.4 shows SEM image of the trench profile after the oxide was etched.

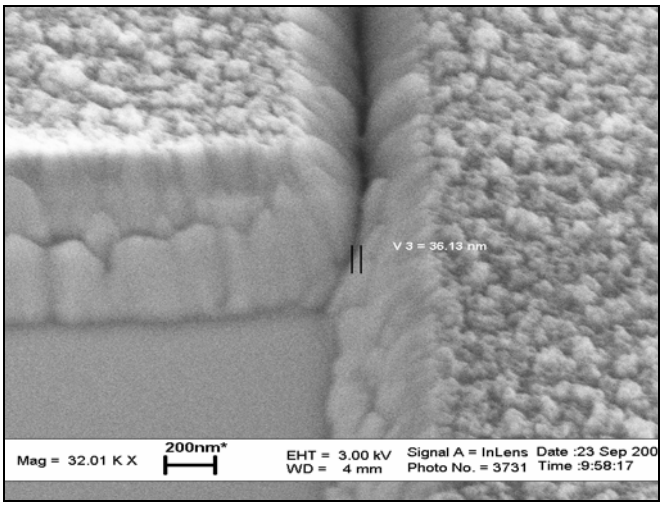


Figure 5.4: SEM image of the trench profile after oxide etching

5.3 Silicon etching in standard Bosch process using STS ICP

The standard Bosch process is composed of a passivation step and an etching step. During the passivation step, C_4F_8 gas is used to passivate the sidewall and prevent lateral etching in the etch step. Then, SF_6 gas is used to etch the silicon in the etching step. Since SF_6 gas etches silicon in an isotropic manner, a RF bias is used to accelerate the SF_6 gas toward the substrate to give a more anisotropic profile. In addition, Ar gas may be added during the etching step to help remove some of the passivation layer at the bottom of the trench. The passivation and etching cycle repeat until the desired depth is etched.

There are many challenges for sub-100nm wide trench etching. For example, the lateral undercut during the etching step will cause the trench to widen and prevent achieving smaller gap. Furthermore, as the gap opening becomes narrower, there may not be enough plasma to reach the bottom of the trench, and no more etching will take place.

In order to achieve high anisotropy and high-aspect ratio etching, it is important to understand the mechanism for reduced sidewall reaction, sidewall passivation technique, aspect ratio dependent etching (RIE lag effect), micro loading, and grass formation. This work aimed to investigate the effect of different parameters in plasma etching at the nanoscale domain.

In general, there are three ways to achieve high aspect-ratio nano trench. First, increase the switching frequency of the plasma gases while keeping the cycle time ratio of etching to passivation constant (e.g. reduce the passivation and etching cycle time from 4 seconds to 3 seconds). This will reduce the sidewall roughness by decreasing the isotropic etch time at the bottom of the trench before the next passivation step protects the sidewall.

Second, increase the platen power to generate more plasma. This will intensify the plasma ions density and energy, and improve the directionality of the plasma reactive particles. Moreover, this will also enhance the availability of plasma species at the bottom of a trench when the opening is too narrow for the plasma to get inside. However, too much increase in platen power will cause bowing in the trench profile. To overcome this problem, some oxygen could be added in SF_6 plasma to eliminate bowing.

Third, reduce the chamber pressure. This will increase the mean free path between the plasma ions and improve the directionality of energetic ions toward the target surface. However, reducing the chamber pressure below a certain point will also decrease the total number of plasma ions available in the chamber. The ions may recombine before they have a chance to reach the target, and no etching will occur.

To study the effect of different parameters, a series of characterization were performed and presented. Table 5.4 provides the detail information of a standard silicon etching recipe as a reference for comparison with the effect of varying different parameters.

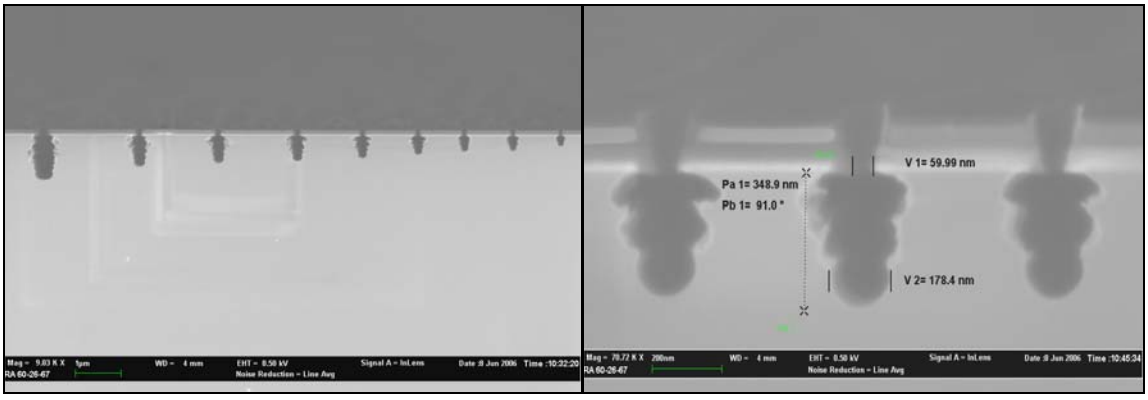
Table 5.4 Detail information of a standard silicon etching recipe

Total # of cycle	Pass/Etch time (sec)	Pressure (mT)	RF platen power Etch/Pass (W)	Etch SF_6/O_2 (sccm)	Passivation C_4F_8 (sccm)	RF bias power Etch/Pass (W)
5	3/5	10	30/0	130/13	100	800/600

1. Effect of etching and passivation time per cycle (3sec passivation and 5sec etching versus 4sec passivation and 4sec etching)

In the first characterization test, the effect of etching time versus passivation time was investigated. The total time in each etching/passivation cycle was 8 seconds, while the etching and passivation time in each cycle were varied. One sample was etched using 3 seconds passivation and 5 seconds etching per cycle, and the other sample was etched using 4 seconds passivation and 4 seconds etching. Figure 5.5 shows SEM images of the resulting trench profile.

3s passivation, 5s etch



4s passivation, 4s etch

Figure 5.5: SEM images of silicon trench profile showing the effect of etching versus passivation time

It was observed that 5 seconds etching time resulted in deeper etching (349nm deep) than the 4 seconds etching time (206nm deep). However, uneven etch could be seen in the trench profile with longer etching time. This was most likely due to insufficient time for passivation to cover the sidewall during the etching. A more uniform profile was observed when the etching and passivation time in each cycle were matched. Therefore, one should use equal etching and passivation to obtain more uniform sidewall profile.

2. Effect of process pressure (8mT versus 10mT)

The second characterization test involved varying the process pressure from 8mT to 10mT. Figure 5.6 shows SEM images of the resulting trench profile.

8mT

10mT

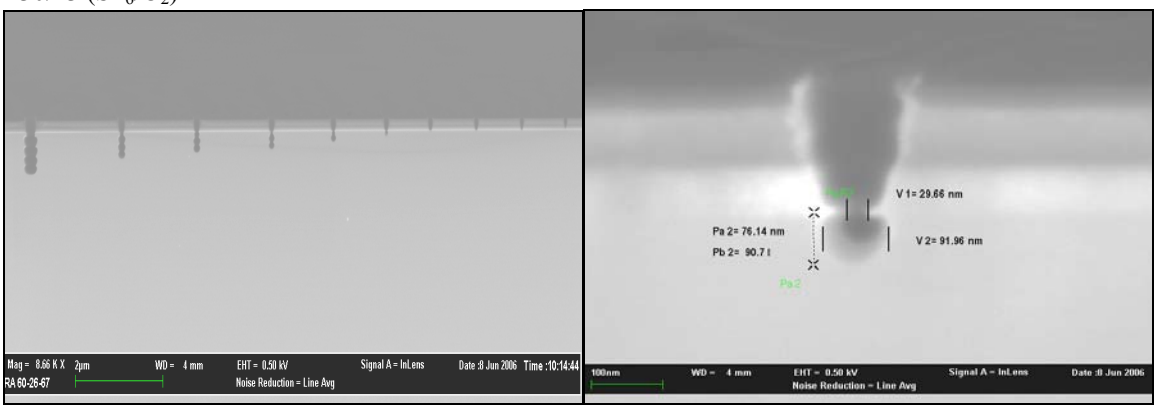
Figure 5.6: SEM images of silicon trench profile showing the effect of process pressure

No significant difference was observed between 8mT and 10mT process pressure. The minimum feature obtained from both samples was 29nm wide and 80nm deep.

3. Effect of SF_6/O_2 gas flow rate (130/13 versus 110/30)

The third characterization test involved varying the ratio of SF_6 to O_2 gas flow rate. One sample had 130sccm SF_6 and 13sccm O_2, and the other sample had 110sccm SF_6 and 30sccm O_2. Figure 5.7 shows SEM images of the resulting trench profile.

130/13 (SF_6/O_2)



110/30 (SF_6/O_2)

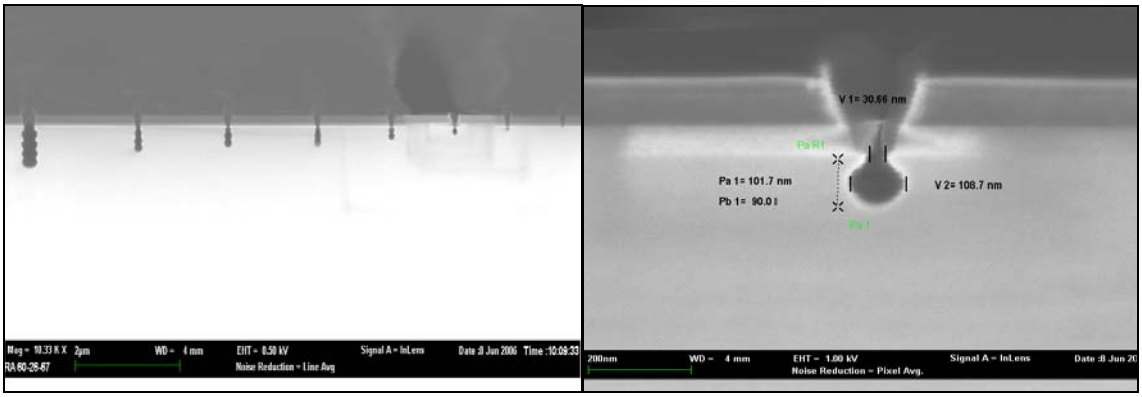


Figure 5.7: SEM images of silicon trench profile showing the effect of SF6/O2 gas flow rate

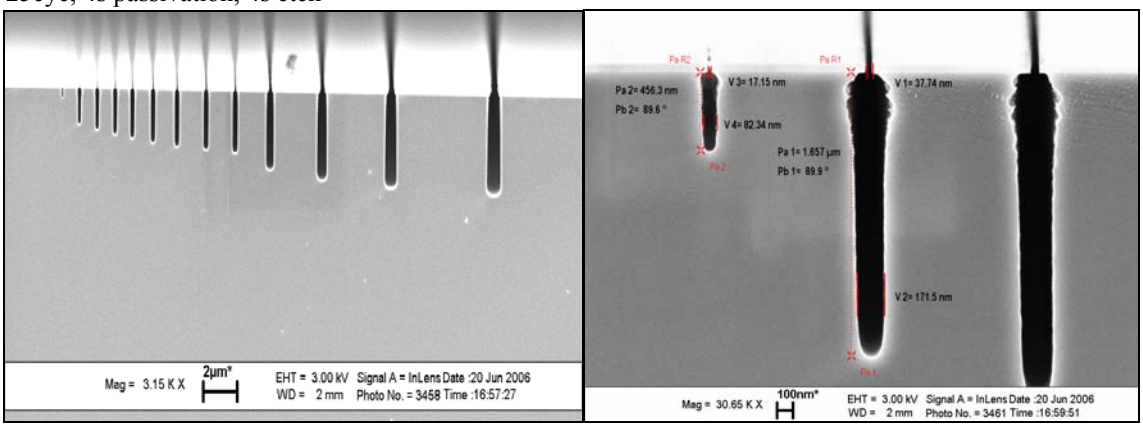
It was observed that higher O_2 concentration (20%, 110/30) resulted in less lateral undercut than lower O_2 concentration (10%, 130/13). The minimum etched hole from the higher O_2 concentration also seemed more rounded.

4. Effect of etching and passivation time at longer cycles (4sec passivation and 4sec etching versus 5sec passivation and 3sec etching)

The fourth characterization test involved etching for longer cycles and varying the etching and passivation time per cycle. One sample was etched for 25 cycles using 4 seconds passivation and 4 seconds etching per cycle, and the other sample was etched for

27 cycles using 5 seconds passivation and 3 seconds etching. Figure 5.8 shows SEM images of the resulting trench profile.

25cyc, 4s passivation, 4s etch



27cyc, 5s passivation, 3s etch

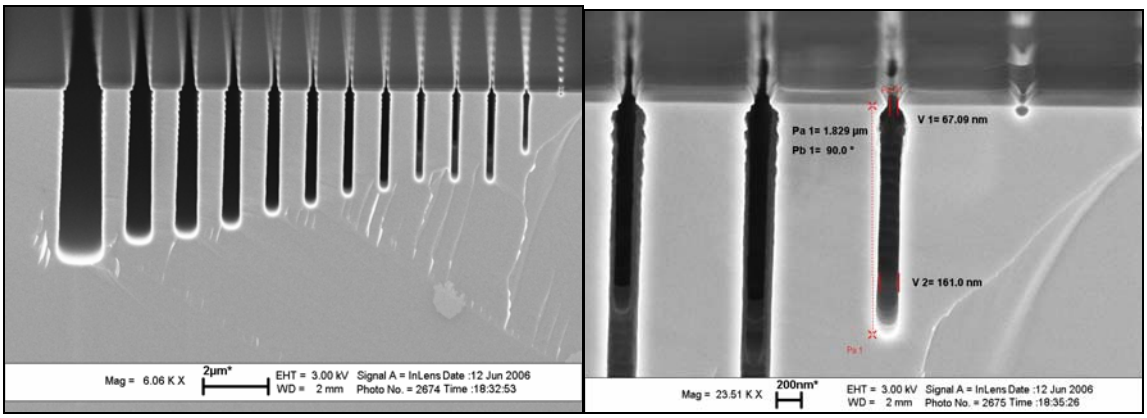


Figure 5.8: SEM images of silicon trench profile showing the effect of etching and passivation time at longer cycles

The smallest trench obtained from the sample with matched etching and passivation time per cycle was 171nm-wide, 1.657um-deep with aspect-ratio of 10, and the smallest trench obtained from the sample with 5 seconds passivation and 3 seconds etching was 161nm-wide, 1.829um-deep with aspect-ratio of 11.

5. Effect of etching for longer number of cycles (10cycles versus 20cycles)

The fifth characterization test involved varying the total etching cycles from 10 cycles to 20 cycles using the standard recipe. Figure 5.9 shows SEM images of the resulting trench profile.

10cycles 20cycles

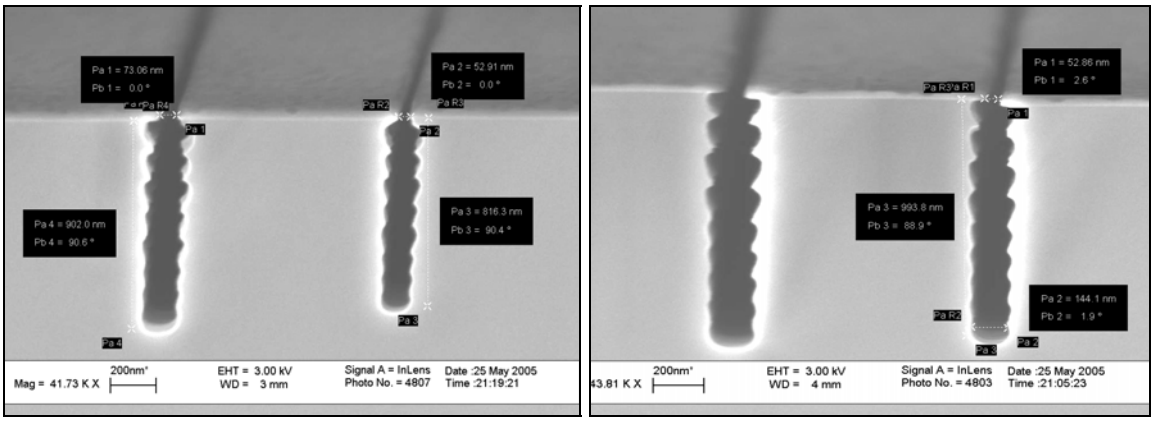


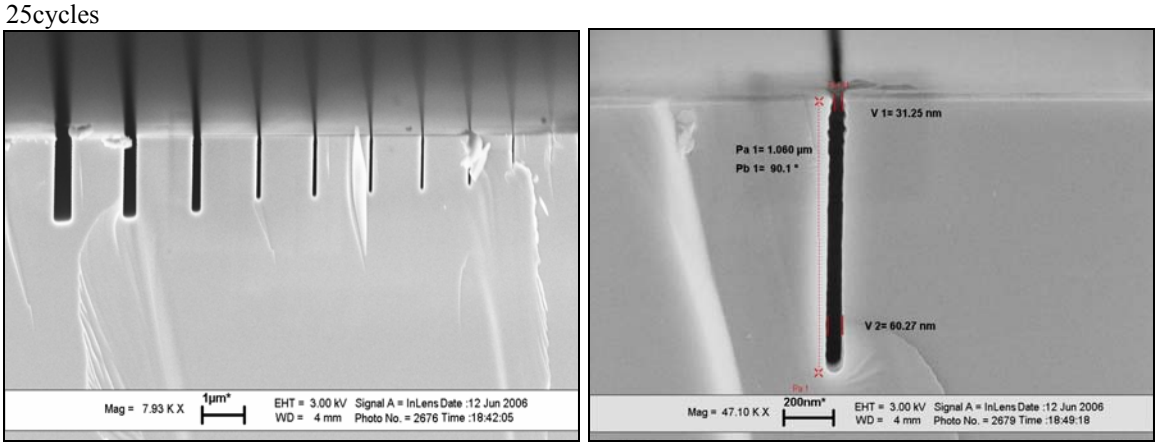
Figure 5.9: SEM images of silicon trench profile showing the effect of etching for longer cycles

The first sample resulted in 816nm-deep trench, and the second sample resulted in 993nm-deep trench. The gap openings in both samples were 53nm-wide, and the trench widths were also comparable. The small increase in the trench depth indicated that etching had stopped, and to etch deeper trench was not possible.

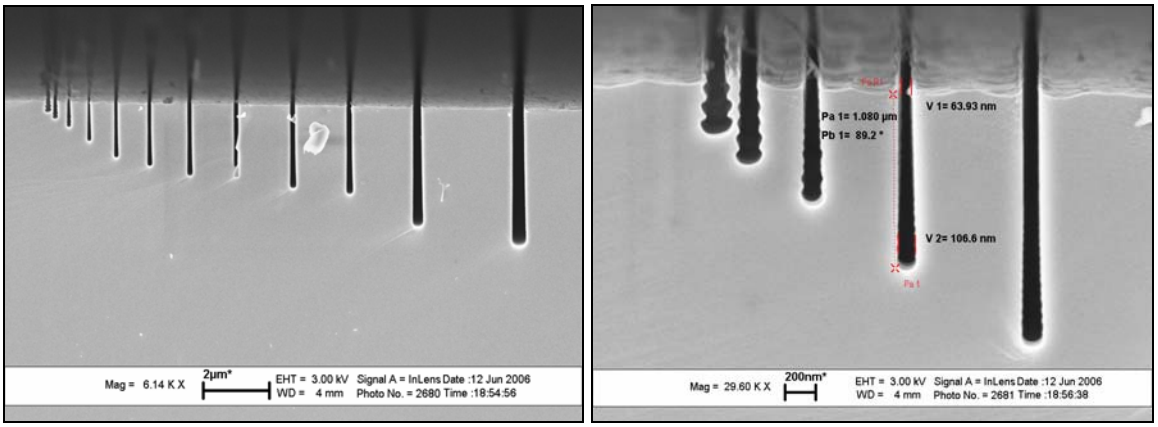
6. Effect of etching for longer number of cycles with different SF_6/O_2 ratio (25, 50 and 100 cycles)

The sixth characterization test involved etching the sample with different SF_6/O_2 ratio (110/30) for longer cycles. The first sample was etched for 20 cycles, the second sample was etched for 50 cycles, and the third sample was etched for 100 cycles. Figure 5.10 shows SEM images of the resulting trench profile.

25cycles



50cycles



100cycles

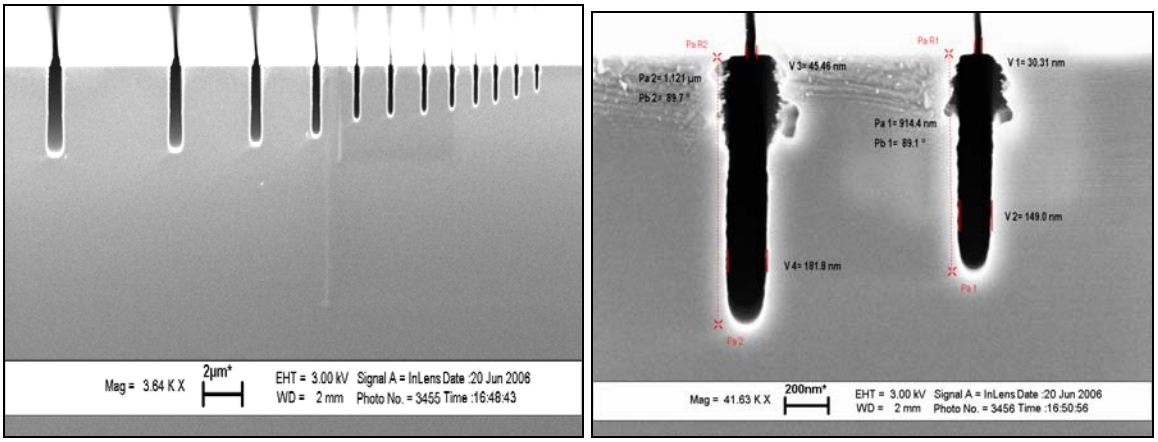


Figure 5.10: SEM images of silicon trench profile showing the effect of etching for longer cycles with different SF_6/O_2 ratio

The smallest trench obtained from 25 cycles of etching was 60nm-wide, 1.06um-deep with aspect-ratio of 17; the smallest trench resulted from 50 cycles of etching was 106nm-wide, 1.08um-deep with aspect-ratio of 10; and the smallest trench resulted from 100 cycles of etching was 149nm-wide, 914nm-deep with aspect-ratio of 6. It was observed that with longer cycles of etching, the aspect-ratio decreased and the minimum trench width increased. This was due to the lateral undercut at longer cycles of etching. Table 5.5 summarizes the effect of varying different parameters.

Table 5.5 Summary of the effect of different parameter

Recipe #	Total # of cycle	Passivation time (s)	Etching time (s)	Pressure (mTorr)	SF6/O2 flow (sccm)	RF platten power Etch/Pass (W)	RF generator power Etch/Pass (W)	AR	Minimum width (nm)
1	5	**3**	**5**	10	130/13	30/0	800/600	n/a	n/a
2	5	**4**	**4**	10	130/13	30/0	800/600	n/a	n/a
3	5	4	3	**10**	130/13	30/0	800/600	n/a	n/a
4	5	4	3	**8**	130/13	30/0	800/600	n/a	n/a
5	5	4	3	8	**110/30**	30/0	800/600	n/a	n/a
6	**25**	**4**	**4**	10	130/13	40/0	800/600	19	105
7	**27**	**5**	**3**	10	130/13	40/0	800/600	11	161
8	**10**	5	4	10	130/13	30/0	800/600	n/a	n/a
9	**20**	5	4	10	130/13	30/0	800/600	7	144
10	**25**	4	3	8	**110/30**	30/0	800/600	17	60
11	**50**	4	3	8	**110/30**	30/0	800/600	10	106
12	**100**	4	3	8	**110/30**	30/0	800/600	6	149

5.4 Silicon etching in modified three-pulse Bosch process

After investigating the effect of changing different process parameters in the STS ICP system, a modified three-pulse Bosch process was developed in the plasma ICP, where a depassivation step was added between the passivation and etching step. In this process, the depassivation step removed some of the passivation layer inside the trench without introducing the SF6 etching gas at the same time, while in the regular Bosch

process, the depassivation step occurred with the etching step simultaneously. This additional step allowed for more control of the etching process by making a smoother transition from passivation to etching. Moreover, the Plasma ICP system was preferred over the STS ICP system because the Plasma ICP allowed shorter cycle time (2 seconds) without destabilizing the process. A standard recipe was first developed, and the effect of varying different parameters was characterized. Table 5.6 provides the detail information of the three-pulse silicon etching recipe.

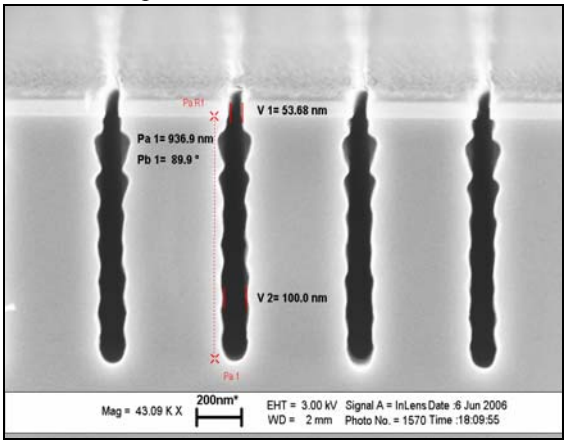
Table 5.6 Detail information of the three-pulse silicon etching recipe

	Passivation				Depassivation				Etch			
Total # of cycle	Time (sec)	pressure (mTorr)	RF1/RF2 (W)	Ar/C4F8 (sccm)	Time (sec)	pressure (mTorr)	RF1/RF2 (W)	O2/Ar (sccm)	Time (sec)	pressure (mTorr)	RF1/RF2 (W)	SF6/Ar (sccm)
10	5	15	1/825	40/70	3	15	18/825	15/45	4	16	15/825	75/5

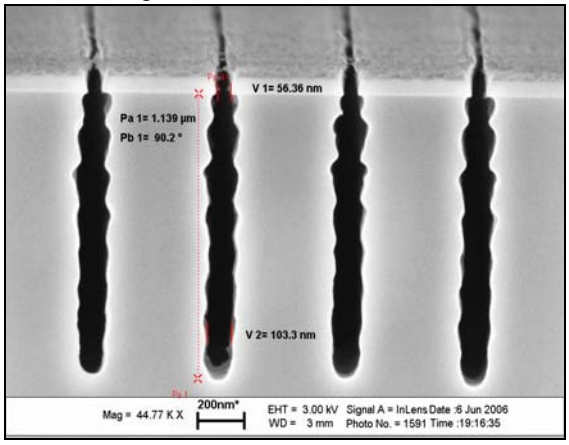
1. Effect of depassivation RF1 power (18W, 21W and 25W)

The first characterization test involved varying the depassivation RF1 power from 18W, 21W to 25W. The RF1 power controls the plasma generation in the Plasma ICP system. Figure 5.11 shows SEM images of the resulting trench profile.

18W RF1 depassivation



21W RF1 depassivation



25W RF1 depassivation

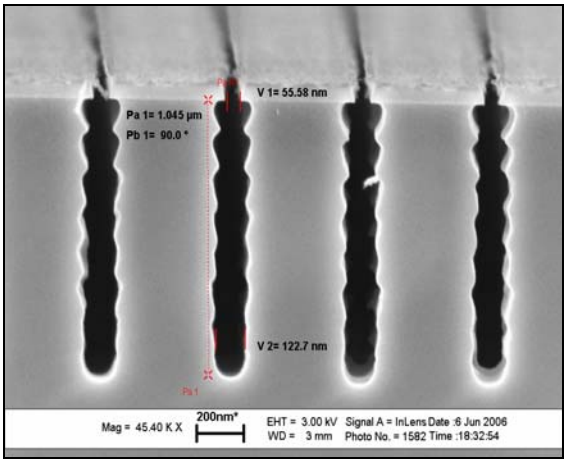


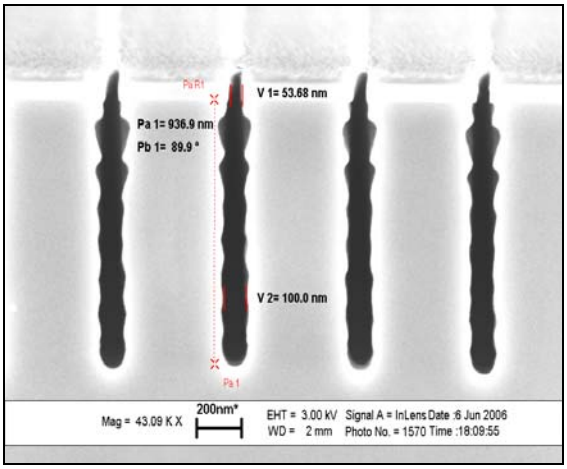
Figure 5.11: SEM images of silicon trench profile showing the effect of RF1 power in depassivation step

The smallest trench resulted from 18W RF1 power was 100nm-wide, 0.936um-deep with aspect-ratio of 9; the smallest trench resulted from 21W RF1 power was 103nm-wide, 1.139um-deep with aspect-ratio of 11; and the smallest trench resulted from 25W RF1 power was 123nm-wide, 1.045um-deep with aspect-ratio of 9. It was observed that 21W RF1 power resulted in the smallest trench with the highest aspect-ratio. The sidewall roughness was also improved by using a lower RF1 power.

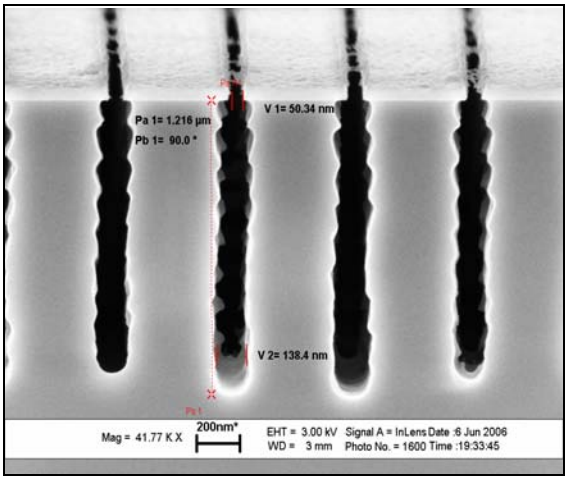
2. Effect of O_2/Ar ratio in depassivation (15/45, 20/40 and 25/35)

The second characterization test involved varying the ratio of O_2/Ar gas flow rate in the depassivation step from 15/45, 20/40 to 25/35 sccm. Figure 5.12 shows SEM images of the resulting trench profile.

15/45 (O_2/Ar)



20/40 (O_2/Ar)



25/35 (O_2/Ar)

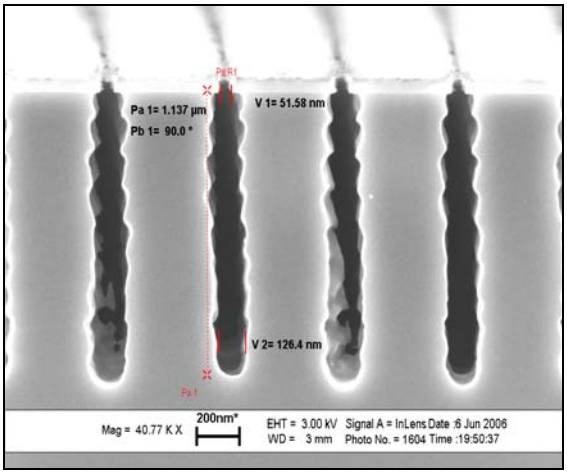


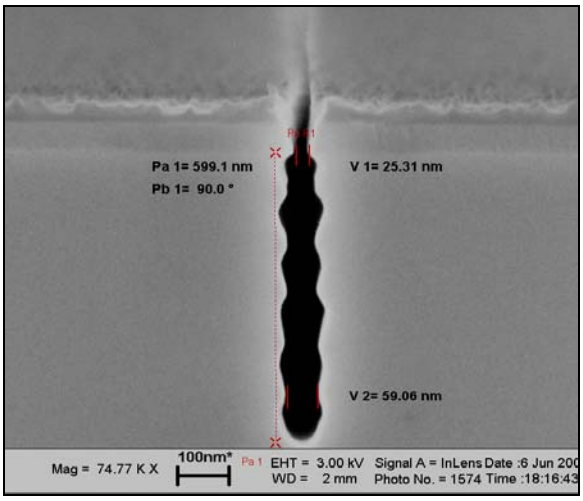
Figure 5.12: SEM images of silicon trench profile showing the effect of the ratio of O_2/Ar gas flow rate in depassivation step

The aspect-ratio was the same in all three samples, while lower O_2 content resulted in smaller gap. O_2 was added to remove the passivation layer. Ar, being a heavier atom, can knock off and loosen some of the passivation layer at the bottom of the trench. The sidewall roughness was improved by using lower O_2 content

3. Effect of depassivation time (3 sec versus 2sec)

The third characterization test involved varying the depassivation time from 2 seconds to 3 seconds. Figure 5.13 shows SEM images of the resulting trench profile.

3sec depassivation



2sec depassivation

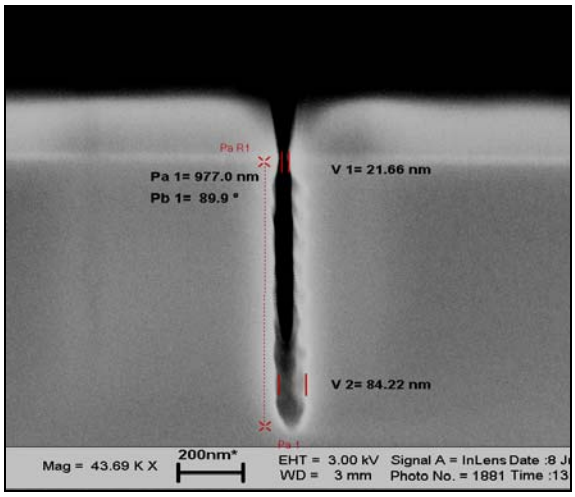


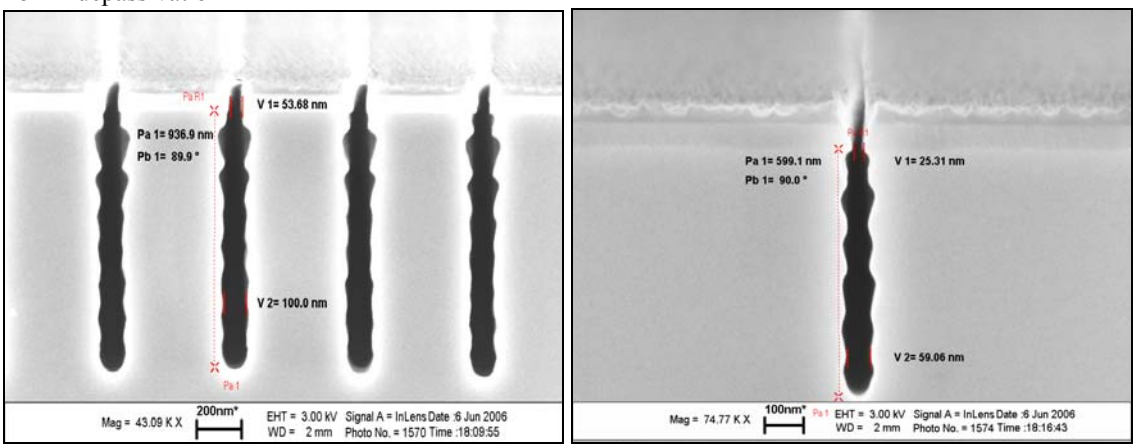
Figure 5.13: SEM images of silicon trench profile showing the effect of depassivation time

The smallest trench resulted from 3 seconds depassivation was 59nm-wide, 0.599um-deep with aspect-ratio of 10; the smallest trench resulted from 2 seconds depassivation was 84nm-wide, 0.977um-deep with aspect-ratio of 12. Since longer depassivation time may also remove some of the passivation layer on the sidewall, the passivation time will also determine the amount of lateral etching that can occur. It was observed that shorter depassivation time resulted in smaller trench.

4. Effect of depassivation pressure (15mT versus 16mT)

The fourth characterization test involved varying the depassivation pressure from 15mT to 16mT. Figure 5.14 shows SEM images of the resulting trench profile.

15mT depassivation



16mT depassivation

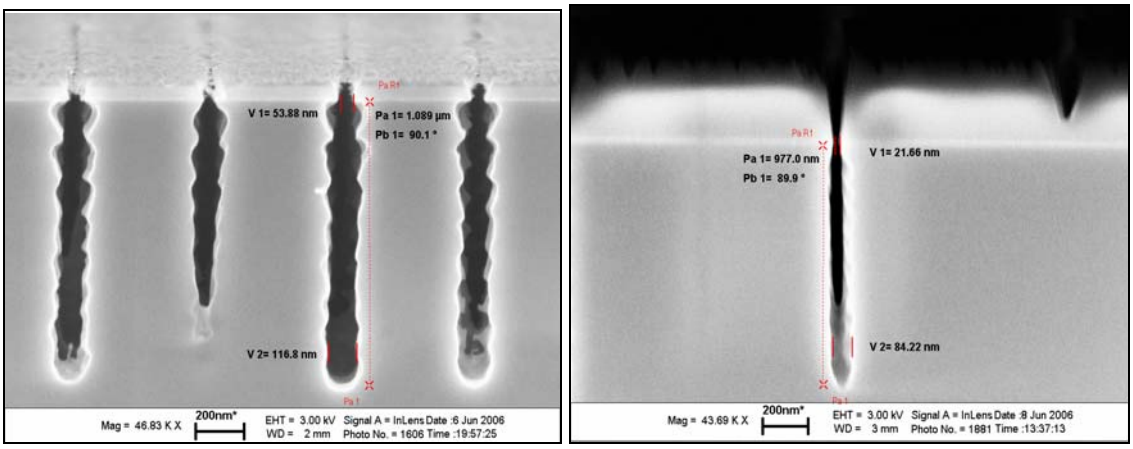


Figure 5.14: SEM images of silicon trench profile showing the effect of depassivation pressure

The smallest trench resulted from 15mT depassivation pressure was 100nm-wide, 0.936um-deep with aspect-ratio of 9; the smallest trench resulted from 16mT depassivation pressure was 117nm-wide, 1.089um-deep with aspect-ratio of 9. Both non-uniform etching and rough sidewall were observed in the 16mT depassivation process.

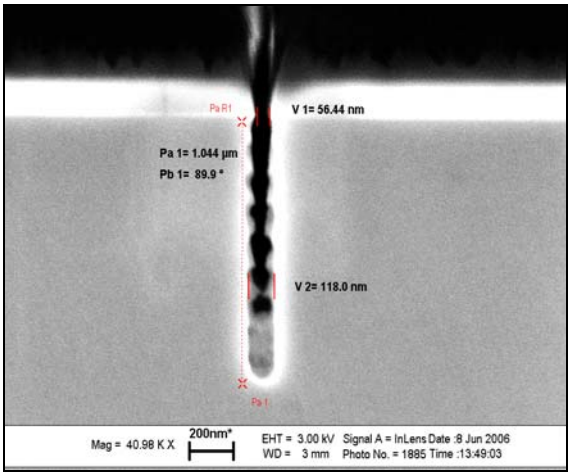
The process pressure usually determines the mean free path inside the chamber. Lower process pressure will result in longer mean free path, which implies that fewer

collisions will occur among the plasma ions. This will result in higher directionality when the plasma ions strike the substrate, and therefore smaller gap.

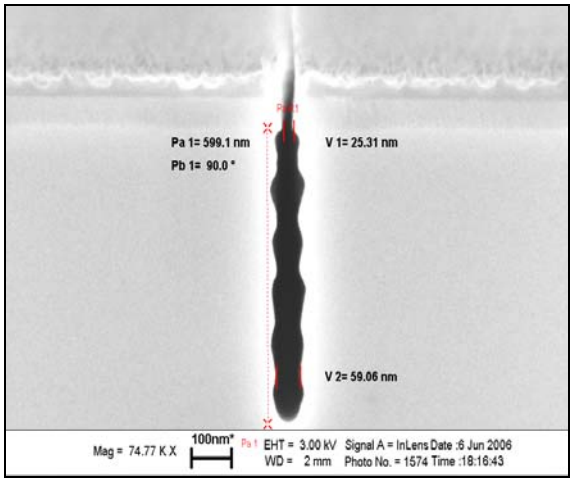
5. Effect of etching pressure (15mT, 16mT and 17mT)

The fifth characterization test involved varying the etching pressure from 15mT, 16mT to 17mT. Figure 5.15 shows SEM images of the resulting trench profile.

15mT etch



16mT etch



17mT etch

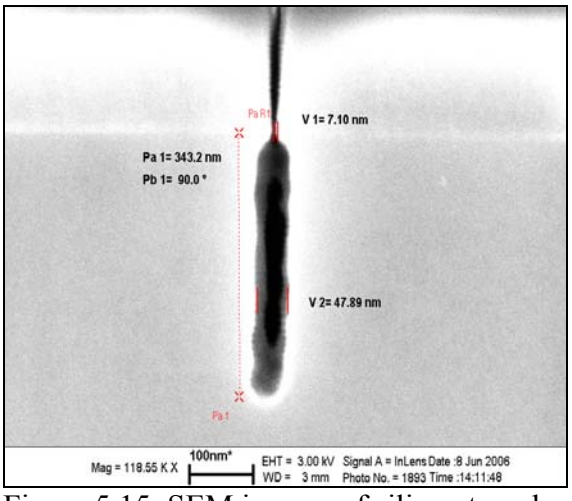


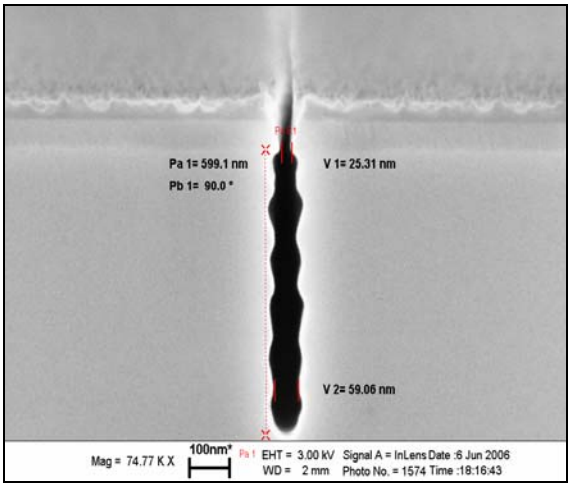
Figure 5.15: SEM images of silicon trench profile showing the effect of etching pressure

The smallest trench resulted from 15mT etching pressure was 118nm-wide, 1.044um-deep with aspect-ratio of 9; the smallest trench resulted from 16mT etching pressure was 59nm-wide, 0.599um-deep with aspect-ratio of 10; and the smallest trench resulted from 17mT etching pressure was 48nm-wide, 0.343um-deep with aspect-ratio of 7. Unlike the effect of depassivation pressure, increasing the etching pressure actually decreased the trench width. However, the aspect-ratio also decreased at higher etching pressure. Therefore, the etching pressure was the optimized at 16mT.

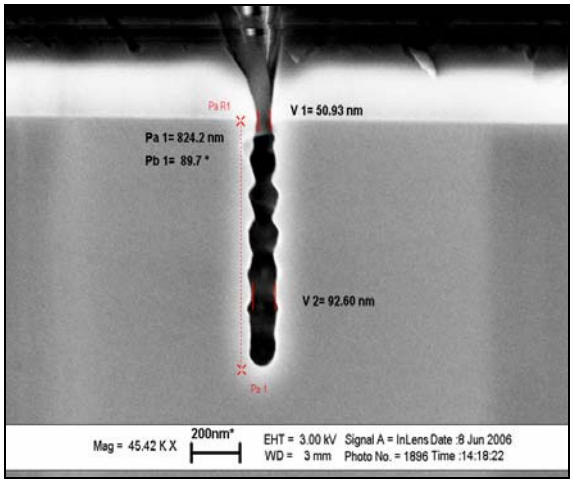
6. Effect of etch RF1 power (15W, 16W and 18W)

The sixth characterization test involved varying the RF1 power in the etching step from 15W, 16W to 18W. Figure 5.16 shows SEM images of the resulting trench profile.

15W RF1 etch



16W RF1 etch



18W RF1 etch

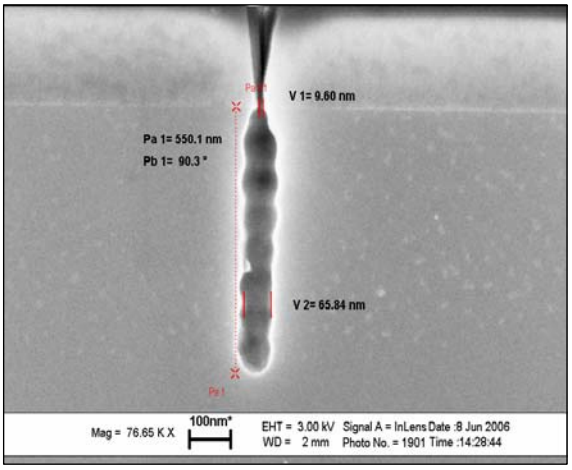


Figure 5.16: SEM images of silicon trench profile showing the effect of RF1 etching power

The smallest trench resulted from 15W RF1 power was 59nm-wide, 0.599um-deep with aspect-ratio of 10; the smallest trench resulted from 16W RF1 power was 93nm-wide, 0.824um-deep with aspect-ratio of 9; and the smallest trench resulted from 18W RF1 power was 66nm-wide, 0.55um-deep with aspect-ratio of 8. It was observed that lower RF1 power resulted in smaller trench and higher aspect-ratio.

The RF1 power controlled the plasma generation. When the RF1 power was raised, more plasma ions were generated and more etching occurred. However, this did not guarantee that the etching was anisotropic. Instead, lateral etching may become more significant and widen the trench gap.

7. Effect of increasing etching cycle with increasing depassivation power and O2/Ar ratio (30 cycles, 35 cycles, 45 cycles, and 80 cycles)

The seventh characterization test involved etching for longer cycles while increasing the depassivation RF1 power from 18-25W at 3W increment for every 30

cycles of etching. Figure 5.16 to 5.19 are SEM images of the trench profile from various etching cycles.

30 etching cycles

28nm-wide 700nm-deep (AR:25), 76nm-wide1.551um-deep (AR:20)

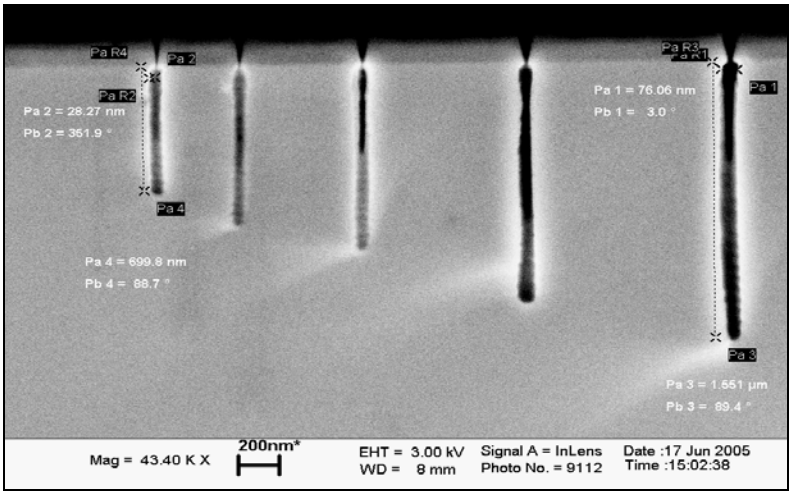


Figure 5.17: SEM images of silicon trench profile after 30 cycles of etching

35 etching cycles

54nm-wide 1.03um-deep (AR:19), 68nm-wide 1.557um-deep (AR:22.5)

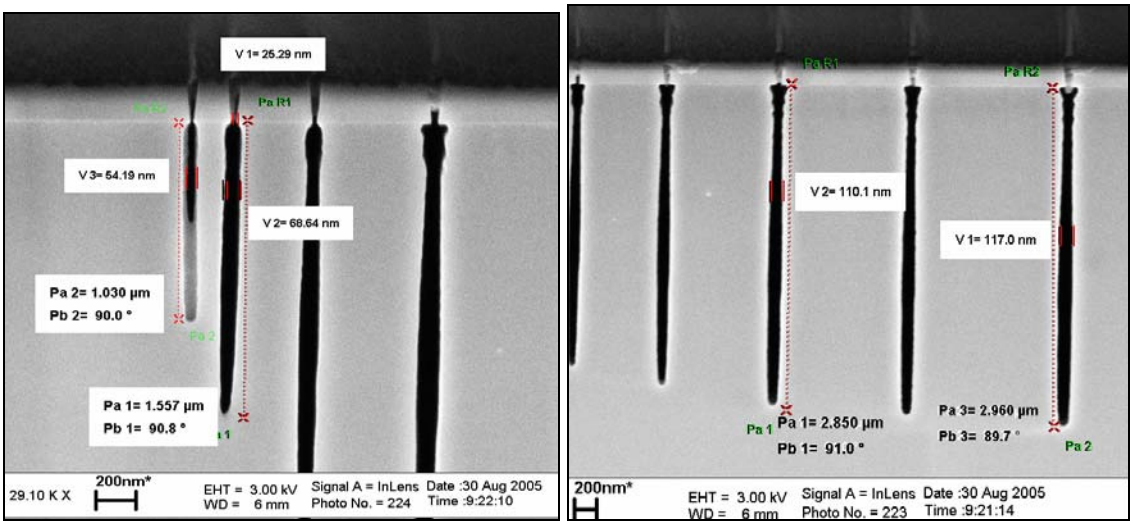
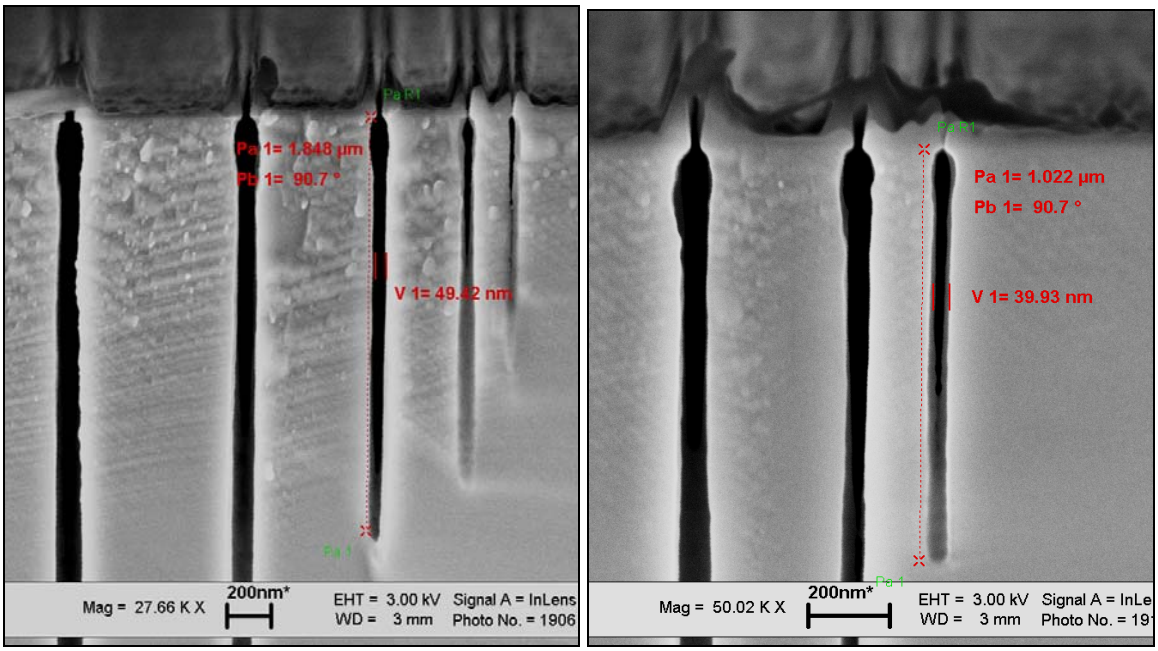


Figure 5.18: SEM images of silicon trench profile after 35 cycles of etching

45cycles etching

49nm-wide 1.848um-deep (AR:37), 40nm-wide 1.022um-deep (AR:25)



139nm-wide 2.464um-deep (AR:18)
46nm-wide 1.262um-deep (AR:27)

60nm-wide 803nm-deep (AR:13)
40nm-wide 572nm-deep (AR:14)

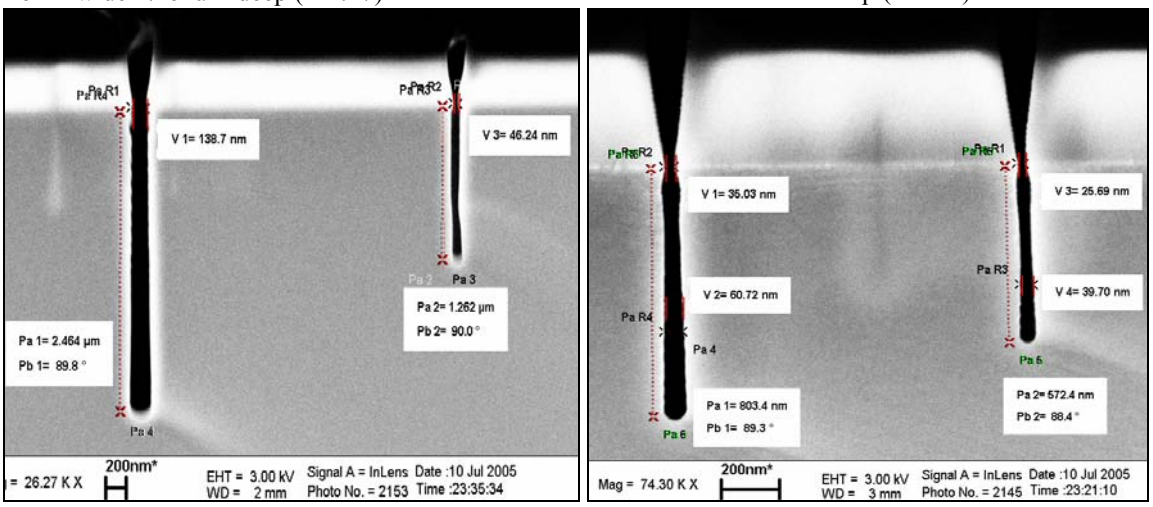
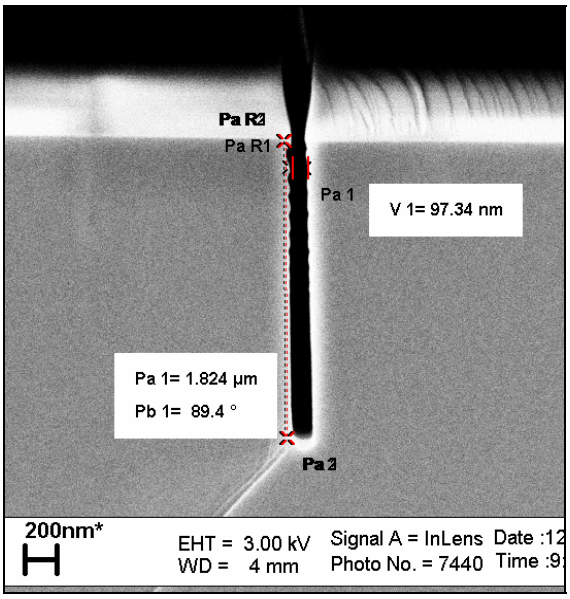


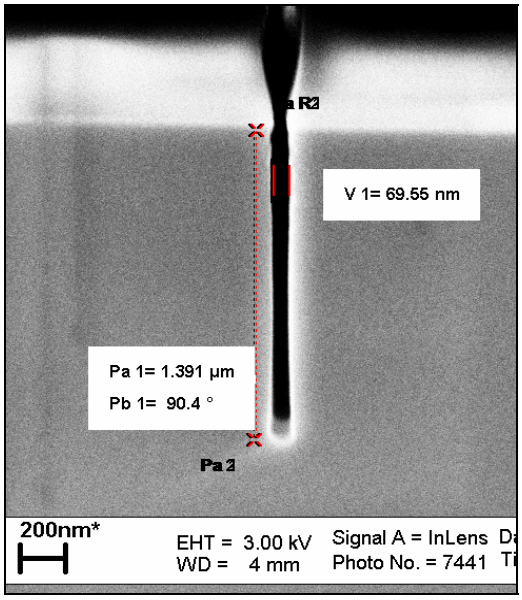
Figure 5.19: SEM images of silicon trench profile after 45 cycles of etching

80cycles etching

97nm-wide 1.824um-deep (AR:15)



70nm-wide 1.391um-deep (AR:15)



49nm-wide 793nm-deep (AR:16)

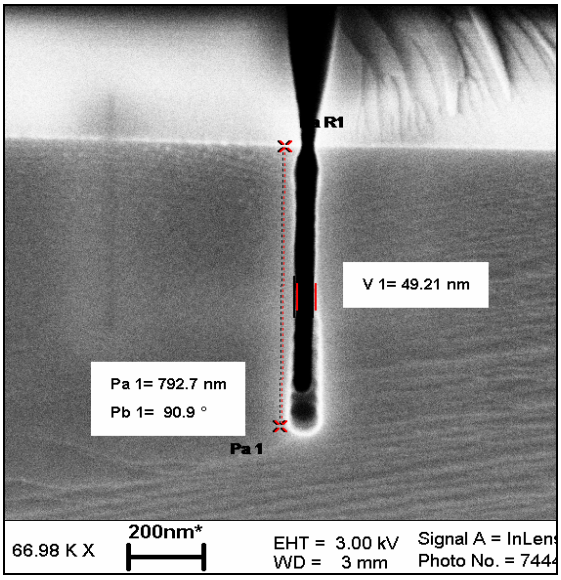


Figure 5.20: SEM images of silicon trench profile after 80 cycles of etching

The smallest trench obtained was 28nm-wide trench with aspect-ratio of 25 from 30 cycles of etching. The highest aspect-ratio obtained was 50nm-wide trench with

aspect-ratio of 37 from 45 cycles of etching. Table 5.7 summarizes the effect of different process parameters.

Table 5.7 Summary of the effect of different parameter

Recipe number	Total number of etching cycle	Passivation				Depassivation				Etch				Minimum width (nm)	AR
		Time (sec)	pressure (mTorr)	RF1/RF2 (W)	Ar/C_4F_8 (sccm)	Time (sec)	pressure (mTorr)	RF1/RF2 (W)	O_2/Ar (sccm)	Time (sec)	pressure (mTorr)	RF1/RF2 (W)	SF_6/Ar (sccm)		
1	10	5	15	1/825	40/70	3	15	**18**/825	15/45	4	16	15/825	75/5	60	10
2	10	5	15	1/825	40/70	3	15	**21**/825	15/45	4	16	15/825	75/5	103	11
3	10	5	15	1/825	40/70	3	15	**25**/825	15/45	4	16	15/825	75/5	123	9
4	10	5	15	1/825	40/70	3	15	18/825	**20/40**	4	16	15/825	75/5	138	9
5	10	5	15	1/825	40/70	3	15	18/825	**25/35**	4	16	15/825	75/5	126	9
6	10	5	15	1/825	40/70	3	**16**	18/825	15/45	4	16	15/825	75/5	117	9
7	10	5	15	1/825	40/70	**2**	15	18/825	15/45	4	16	15/825	75/5	84	12
8	10	5	15	1/825	40/70	3	15	18/825	15/45	4	**15**	15/825	75/5	118	9
9	10	5	15	1/825	40/70	3	15	18/825	15/45	4	**17**	15/825	75/5	48	7
10	10	5	15	1/825	40/70	3	15	18/825	15/45	4	16	**16**/825	75/5	93	9
11	10	5	15	1/825	40/70	3	15	18/825	15/45	4	16	**18**/825	75/5	66	8
12	**30**	5	15	1/825	40/70	3	15	**18**/825	15/45	4	16	15/825	75/5	28	25
13	**35**	5	15	1/825	40/70	3	15	**18**/825	15/45	4	16	15/825	75/5	54	19
14	**45**	5	15	1/825	40/70	3	15	**18-21**/825	**15/45-20/40**	4	16	15/825	75/5	49	37
15	**80**	5	15	1/825	40/70	3	15	**18-25**/825	**15/45-20/40**	4	16	15/825	75/5	49	16

5.5 Summary of control parameters

Process pressure

In general, decreasing the process pressure will increase the mean free path between the ions in the chamber, resulting in a more anisotropic etching profile. However, decreasing the process pressure too much will reduce the etch rate, because the total number of etching plasma available in the chamber is less. Furthermore, when the process pressure is reduced below a certain level, no etching will occur because the plasma ions will recombine before reaching the substrate. The optimal setting for the

process pressure depends on the chamber size, the total gas flow rate, the gas species, and the RF power to generate the plasma.

Cycle switching time

Although the Bosch process introduces a passivation step to protect the sidewall, SF_6 etching chemistry is mostly isotropic. Therefore, some lateral undercut may still occur during the etching step. It was observed that switching cycle with 5 seconds passivation and 4 seconds etching had more lateral undercut than switching cycle with 4 seconds passivation and 3 seconds etching. Therefore, the switching time between each passivation and etching cycle should be minimized to reduce lateral etching. However, the minimum process time of both the etching and passivation step allowed on the STS ICP system was 3 seconds, below which the system became unstable and the process aborted automatically. For this reason, the Plasma ICP system was used instead, where the minimum allowable process time was 2 seconds.

RF power

In general, there are two RF power sources in the ICP system. The RF platen power (RF1 in Plasma ICP) that controls the plasma generation, and the RF bias power (RF2 in Plasma ICP) that controls the plasma acceleration. A high RF bias power was typically used to increase the anisotropy of the etching. When the RF platen power was low, there may not be sufficient plasma ions generated for etching to occur. Increasing the RF platen power will increase the plasma ion concentration, and therefore resulting in faster etch rate. However, if too many plasma ions were present, some lateral etching may occur. Both the aspect-ratio and the minimum trench width were determined by the RF platen power. For the modified three-pulse process, the same principle applied to both

the depassivation and the etching step. Therefore, one needs to characterize the optimal RF platen power to obtain high-aspect ratio nano-trench.

As the trench becomes deeper, the plasma ions that can reach the bottom of the trench also may become fewer. This will affect both the etch rate and the maximum depth that can be etched. Therefore, for longer cycles of etching, one can modulate the RF1 power (plasma generation) in the three-pulse process to increase the plasma ion concentration as the trench becomes deeper. In the characterization of the three-pulse process, the depassivation RF1 power was increased by 3W after every 30 cycles of etching.

Ratio of O_2/Ar gas flow rate

For the depassivation step in the three-pulse process, O_2 and Ar plasma were introduced together. The function of O_2 plasma was to remove the passivation layer. On the other hand, Argon, being a heavier atom, can sputter and dislodge some passivation layer that could not be removed by O_2 plasma alone. Therefore, the depassivation process could be enhanced by increasing the ratio of O_2 to Ar. This technique was used in conjunction with the RF1 power modulation in the three-pulse process to obtain high aspect-ratio nano trench.

CHAPTER 6

DEVICE FABRICATION AND RESULTS

Various resonator devices have been fabricated using the process developed in this work. These include SiBAR and IBAR. The measurement results are given in the sections below.

6.1 SiBAR/block resonator

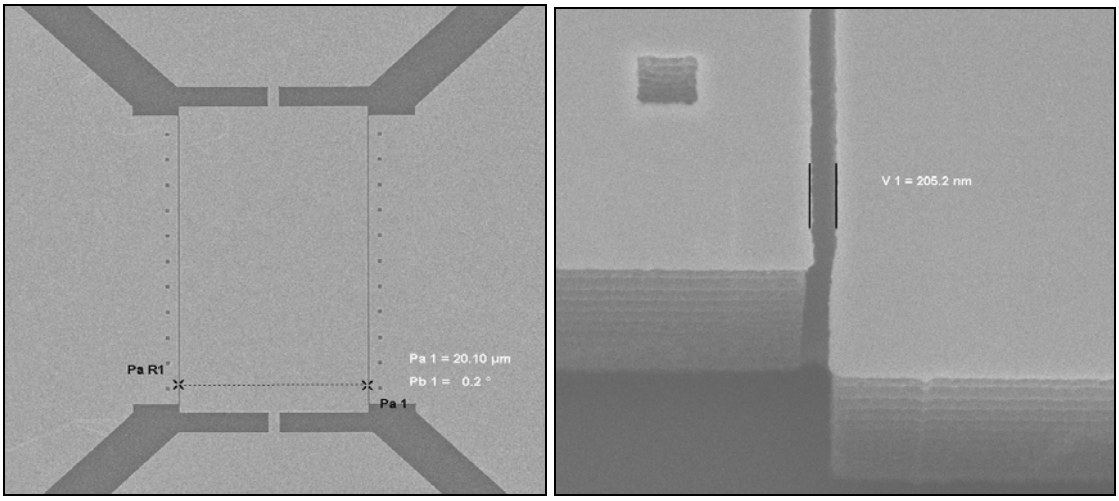
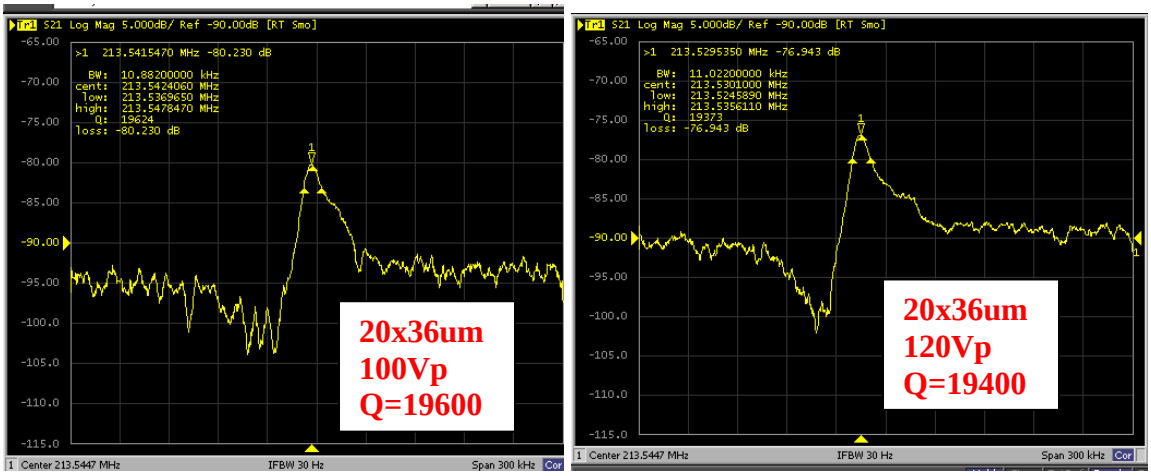


Figure 6.1: SEM image of 20um SiBAR (213MHz)



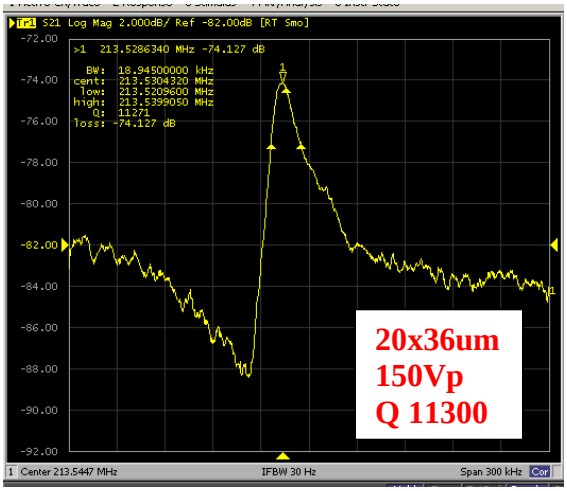


Figure 6.2: Measurement result of 213 MHz SiBAR at 100V, 120V and 150V

105MHz 40um SiBAR

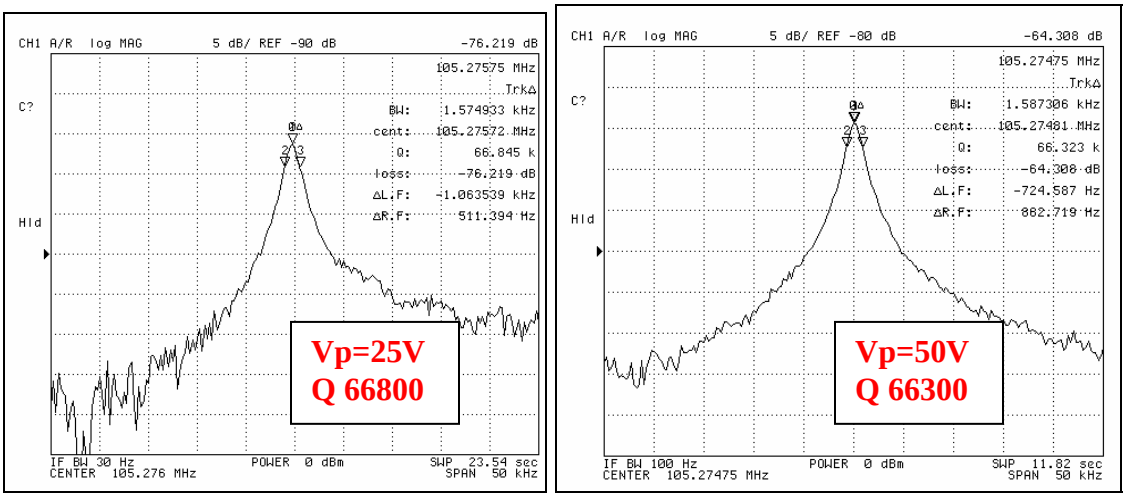


Figure 6.3: Measurement result of 105MHz SiBAR at 25V and 50V

6.2 IBAR

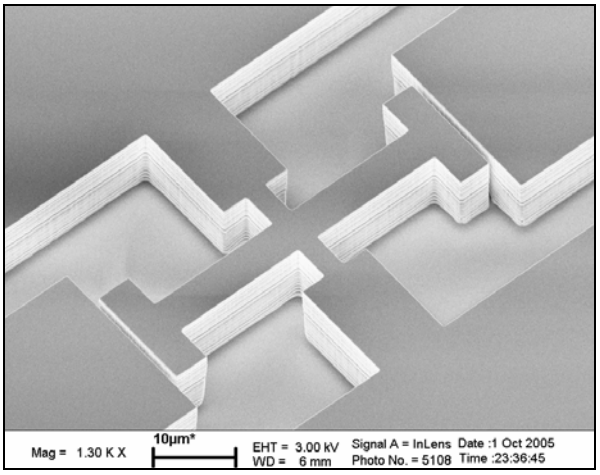


Figure 6.4: Isometric view of 40um IBAR

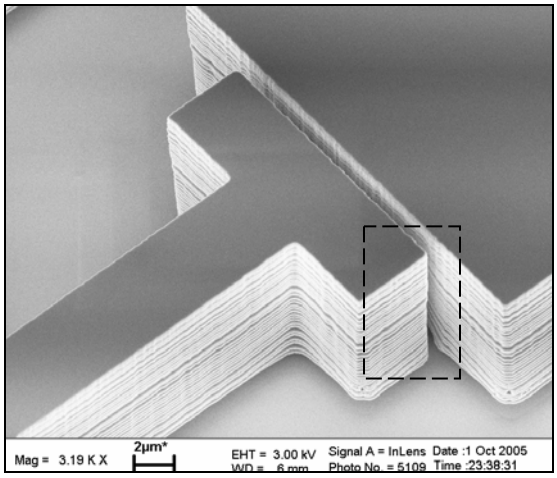


Figure 6.5: Enlarged view of electrode gap

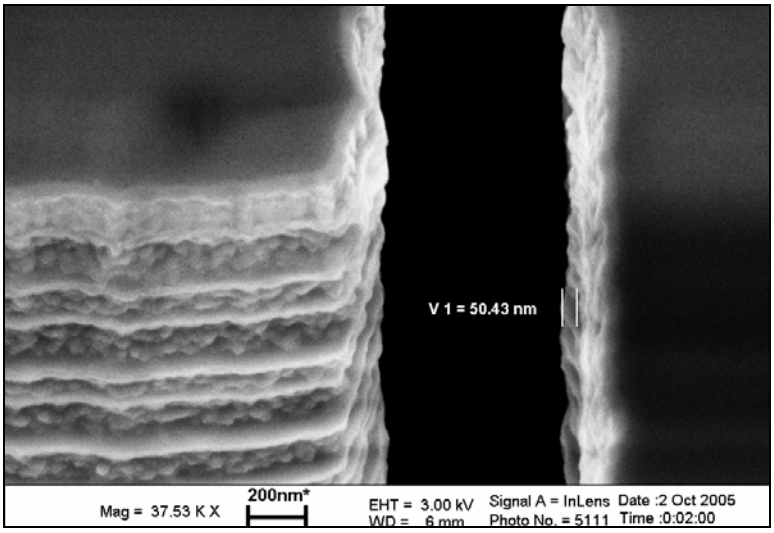


Figure 6.6: Sidewall roughness of electrode gap ~50nm

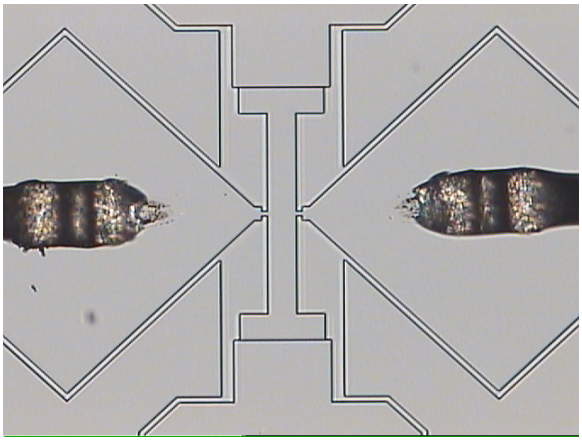


Figure 6.7: Microscope image of tested IBAR

IBAR 15MHz

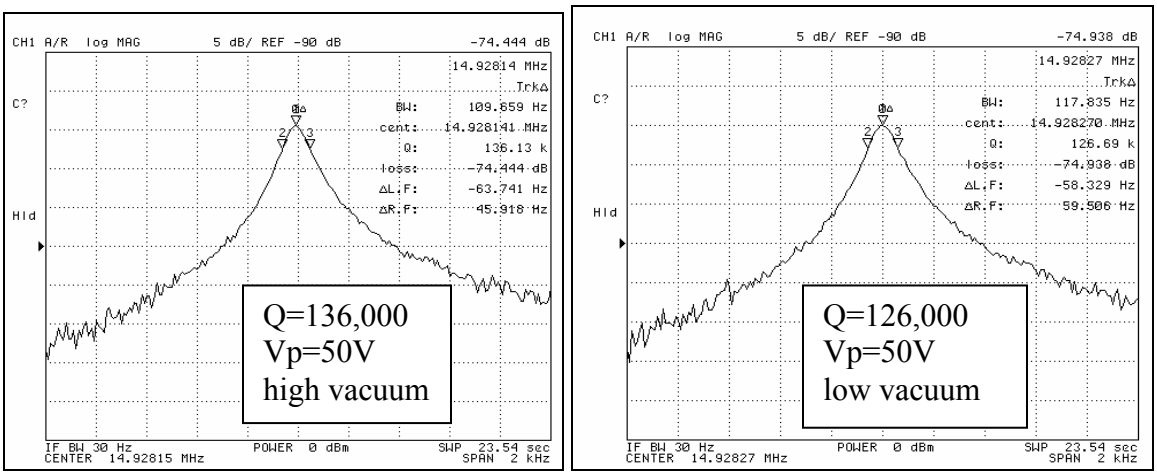
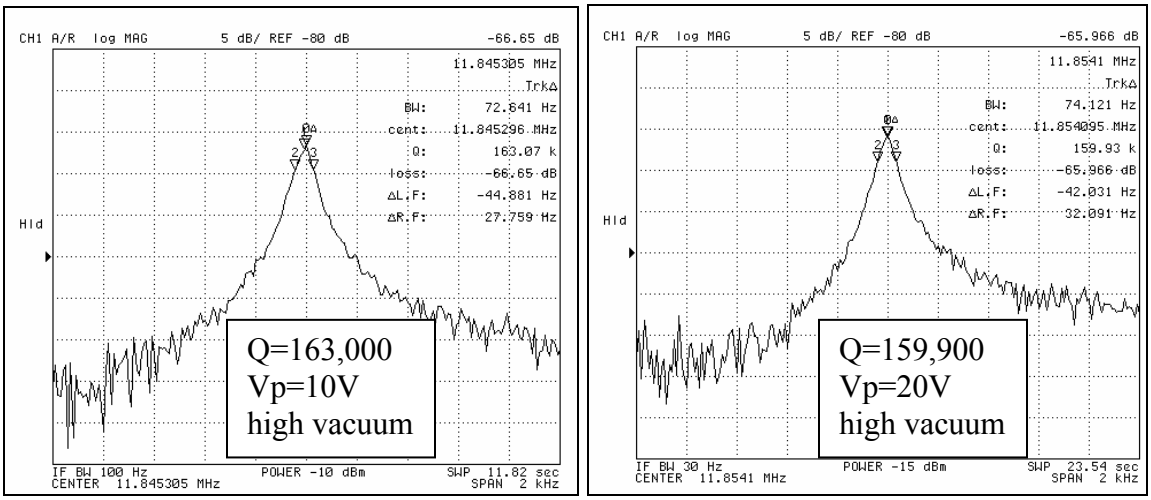


Figure 6.8: Measurement result of 15MHz IBAR at 50V

IBAR 12MHz



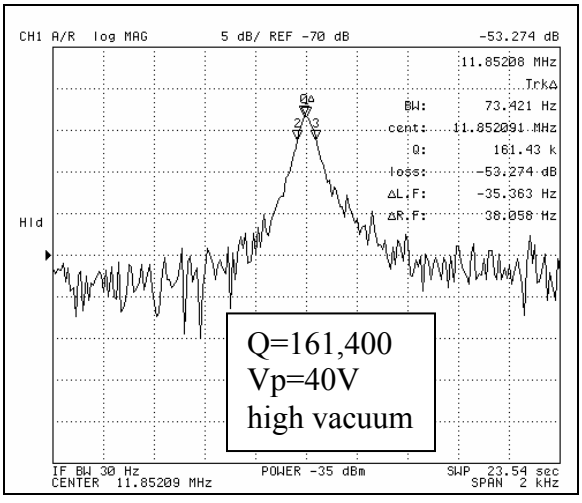


Figure 6.9: Measurement result of 12MHz IBAR at 10V, 20V and 40V

IBAR 6MHz

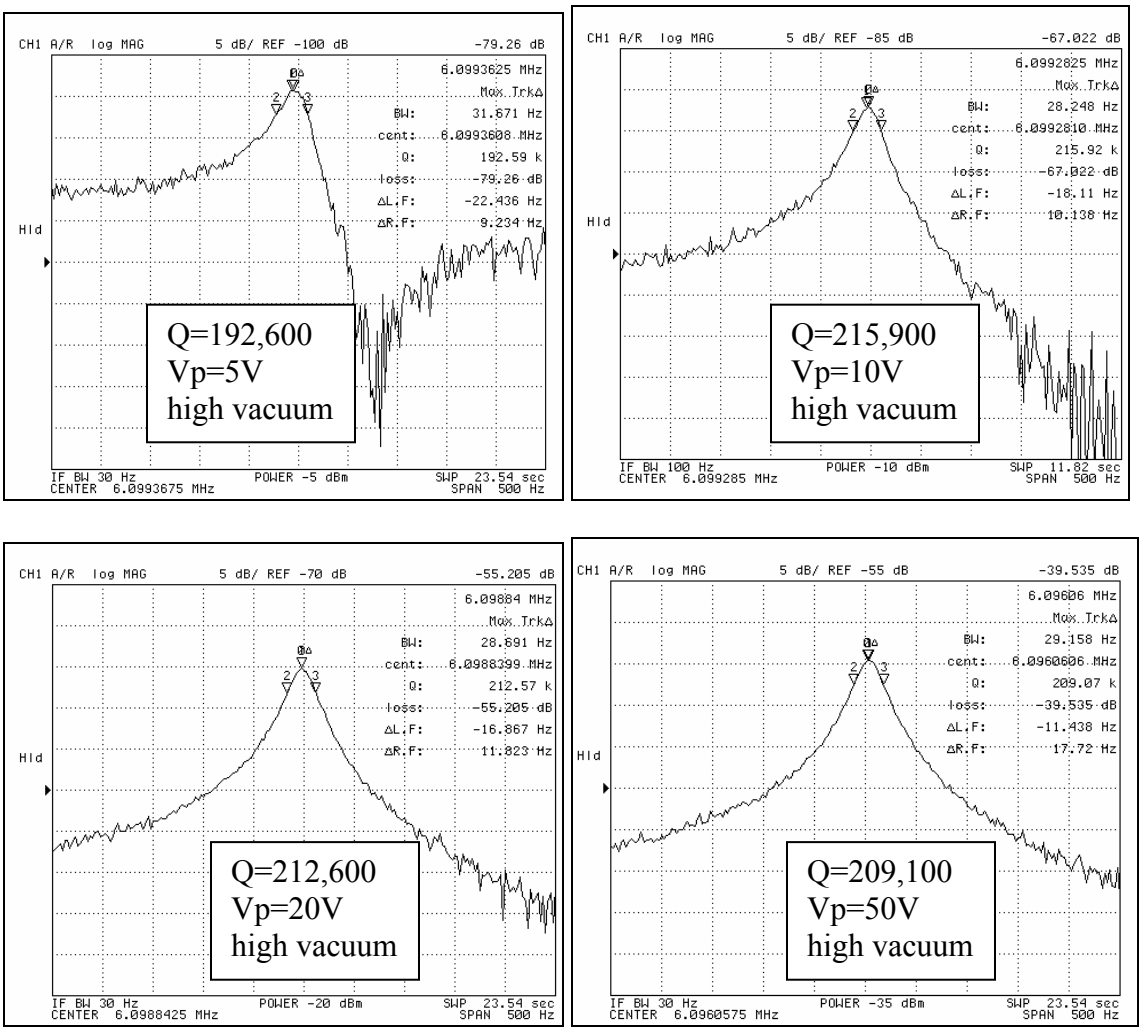


Figure 6.10: Measurement result of 6MHz IBAR at 5V, 10V, 20V and 50V

CONCLUSION

In this work, characterization and development of nanolithography and nanoscale plasma etching were demonstrated. Nanolithography patterning technique using Electron Beam Lithography system was developed. In particular, shot modulation was used to obtain precise dimension in a periodic grating structure. Electron Beam Lithography allowed quick design and test cycle, but its use for large area patterning was limited by long exposure time. In addition, the etching selectivity and exposure time are determined by the resist property.

Nanoscale etching using standard Bosch process and modified three-pulse process were developed and characterized. Various control parameters were investigated and reported also. The characterization of the standard Bosch process showed that the smallest trench obtained was 60nm-wide with aspect-ratio less than 20. On the other hand, using the modified three-pulse process, the smallest trench obtained was less than 30nm with aspect-ratio of 25. The highest aspect-ratio obtained was 37 for a 50nm-wide trench.

Various resonator devices have been fabricated using the process developed in this work. The measurement results were comparable with the devices fabricated using the HARPSS process. Ultra-high Q (216,900) IBAR devices have been demonstrated. Using the process developed in this work, nanostructure could be fabricated for various other potential applications such as RF filter and biosensor.

APPENDIX A

JOB DECK FILE FOR EBL

```
;-----------------------------------------------------------------
JOB/W  'PERNG11',4      ; 4 inch cassette
;-----------------------------------------------------------------

; This job uses a 200nm thick SOI wafer, with 120nm ZEP on 90nm oxide
; on top of SOI. The goal is to obtain periodic structure by using shot
; modulation

GLMPOS P=(0,33000), Q=(0,-33000)
GLMP 3.0,30.0
GLMQRS 3.0,30.0

       PATH PERNG
              ARRAY   ( -15000,4,10000 )/( 1000,2,3000 )
            CHMPOS M1=(0,0)
            CHMARK 3.0, 30.0
                  ASSIGN P(1) -> ((1,1),MDLT1)
                  ASSIGN P(1) -> ((2,1),MDLT2)
                  ASSIGN P(1) -> ((3,1),MDLT3)
                  ASSIGN P(1) -> ((4,1),MDLT1)
                  ASSIGN P(2) -> ((1,2),MDLT1)
                  ASSIGN P(2) -> ((2,2),MDLT2)
                  ASSIGN P(2) -> ((3,2),MDLT3)
                  ASSIGN P(2) -> ((4,2),MDLT1)
            AEND
      PEND

;-----------------------------------------------------
;       Layer Definition
;-----------------------------------------------------
        LAYER   1
        p( 1 )   '10nm_trench_opto.v30'
        SPPRM 4.0,,,,1.0,1

        p( 2 )   '10trench_opto_bm.v30'
        SPPRM 4.0,,,,1.0,1

        STDCUR 0.1

MDLT1: MODULAT
((0,100),(1,200),(2,0),(3,25),(4,50),(5,100),(6,150),(7,200),(8,100),(9
,100),(10,100))
MDLT2: MODULAT
((0,100),(1,300),(2,0),(3,25),(4,50),(5,100),(6,150),(7,200),(8,100),(9
,100),(10,100))
MDLT3: MODULAT
((0,100),(1,400),(2,0),(3,25),(4,50),(5,100),(6,150),(7,200),(8,100),(9
,100),(10,100))

END
```

APPENDIX B

SCHEDULE FILE FOR EBL

```
MAGAZIN 'PERNG11'

#1
%4A
JDF     'perng11',1
ACC 100
CALPRM '100kv_100pa'
DEFMODE 2       ; 2_stage deflection
RESIST 210      ; Base dose is 210uC/cm2
SHOT A,2


GLMDET M
CHMDET S
CHIPAL 0
HSWITCH OFF,ON

END 1
```

REFERENCES

[1] F. Ayazi, "High-Frequency Integrated Micro-Electro-Mechanical Resonators and Filters," book chapter in *Advanced Micro and Nano Systems*, Vol. 1, pp. 165-192, 2004, Edited by H. Baltes et al, Wiley-VCH.

[2] N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined Inertial Sensors," *Invited paper, Proceedings of the IEEE*, Aug. 1998, pp. 1640-1659.

[3] F. Ayazi and K. Najafi, "High Aspect-Ratio Combined Poly and Single-Crystal Silicon (HARPSS) MEMS Technology," *IEEE Journal of Microelectromechanical Systems*, Vol. 9, Sept. 2000, pp. 288-294.

[4] F. Ayazi, "The HARPSS Process for Fabrication of Precision MEMS Inertial Sensors," *Mechatronics 12 (2002)*, Nov. 2002, pp. 1185-1199, Elsevier Science Ltd.

[5] S. Pourkamali, Z. Hao, and F. Ayazi, "VHF Single Crystal Silicon Elliptic Bulk-Mode Capacitive Disk Resonators; Part II: Implementation and Characterization," *IEEE Journal of Microelectromechanical Systems*, Vol. 13, No. 6, Dec. 2004, pp. 1054-1062.

[6] Z. Hao, A. Erbil, and F. Ayazi, "An Analytical Model for Support Loss in Micromachined Beam Resonators with In-plane Flexural Vibrations," *Sensors and Actuators A*, Vol. 109, Dec. 2003, pp. 156-164.

[7] K. Sundaresan, G.K. Ho, S. Pourkamali, and F. Ayazi, "A Two-Chip, 4-MHz Microelectromechanical Reference Oscillator," *Proc. 2005 IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, Kobe, Japan, May 2005, pp. 5461-5464.

[8] G.K. Ho, K. Sundaresan, S. Pourkamali and F. Ayazi, "Temperature Compensated IBAR Reference Oscillators," *Tech. Dig 19th IEEE International Conference on Micro-Electormechanical Systems Conference 2006 (MEMS 2006)*, Istanbul, Turkey, Jan. 2006, pp. 910-913.

[9] "JBX-9300FS Lithography Operations," http://grover.mirc.gatech.edu/equipment/textInstructions.php?id=156 (Accessed June 2006)

[10] "Proximity Effect in E-Beam Lithography," http://nanolithography.gatech.edu/proximity.htm (Accessed June 2006)

[11] "Electron Beam Lithography Training," http://nanolithography.gatech.edu/JEOL_JBX-9300FS_Training.htm (Accessed June 2006)

[12] "JBX-9300FS General Statements," http://grover.mirc.gatech.edu/equipment/textInstructions.php?id=156 (Accessed June 2006)

[13] T. Yamashita, "Unraveling Photonic Bands: Characterization of Self-Collimation Effects in Two-Dimensional Photonic Crystals," Georgia Institute of Technology Ph.D. Dissertation, 24 May 2005.

[14] Zeon Corporation, "ZEP520 Technical Report," http://www.zeon.co.jp (Accessed June 2006)